

COMPAL CONFIDENTIAL

MODEL NAME :DDM60

PCB NO : LA-F391P

BOM P/N : 431A8K31LXX

BR MLK12 KBL-U UMA

Kabylake U42

2017-09-25

REV:1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

U42@ : KBL-R U42 Component

U22@ : KBL-R U22 Component

DS3@ : Support DS3 Component

NDS3@ : No Support DS3 Component

650@ : Pop NPCT650VB2YX Component

750@ : Pop NPCT750JAAYX Component

MB PCB

Part Number	Description
DAA000EB000	PCB 258 LA-F391P REV0 MB 1

Layout Dell logo



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REV:X00
PWB: 9RJMF

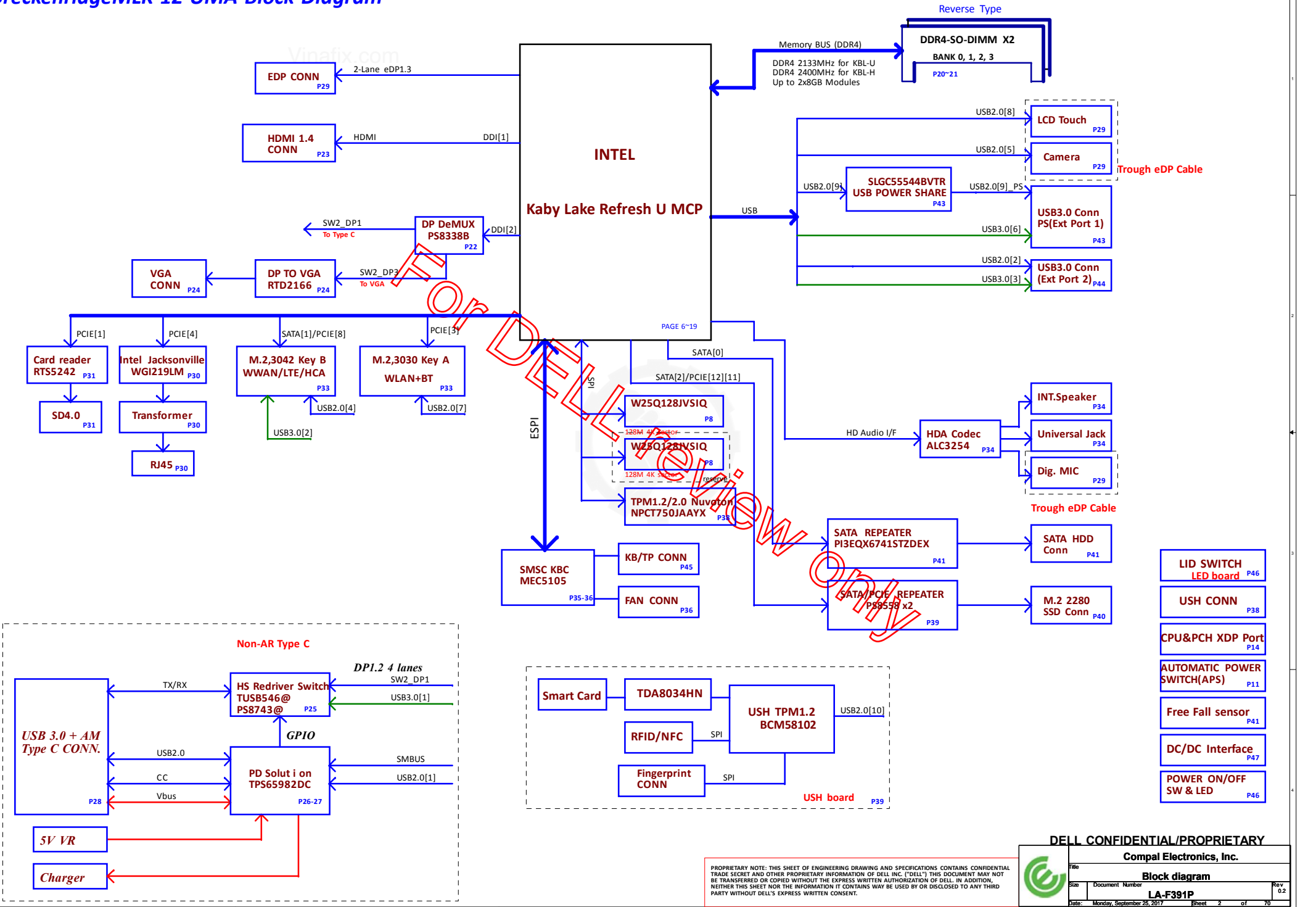
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BreckenridgeMLK 12 UMA Block Diagram



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POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON	ON
S3	ON	ON	OFF	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

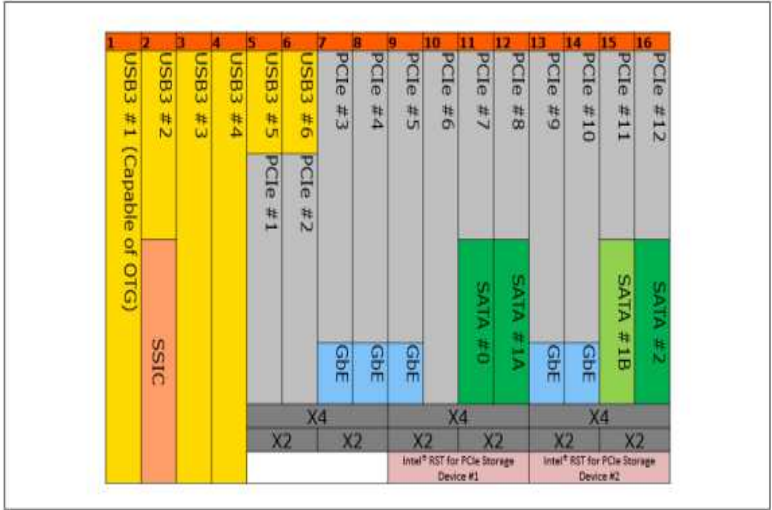
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000 1.211072

For Breckenridge12/14/15 UMA

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Type-C Port
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left
USB3.0-4				JUSB3-->Rear Left
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	M.2 3042(SATA Cache or HCA)
		PCIE-9		NA
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

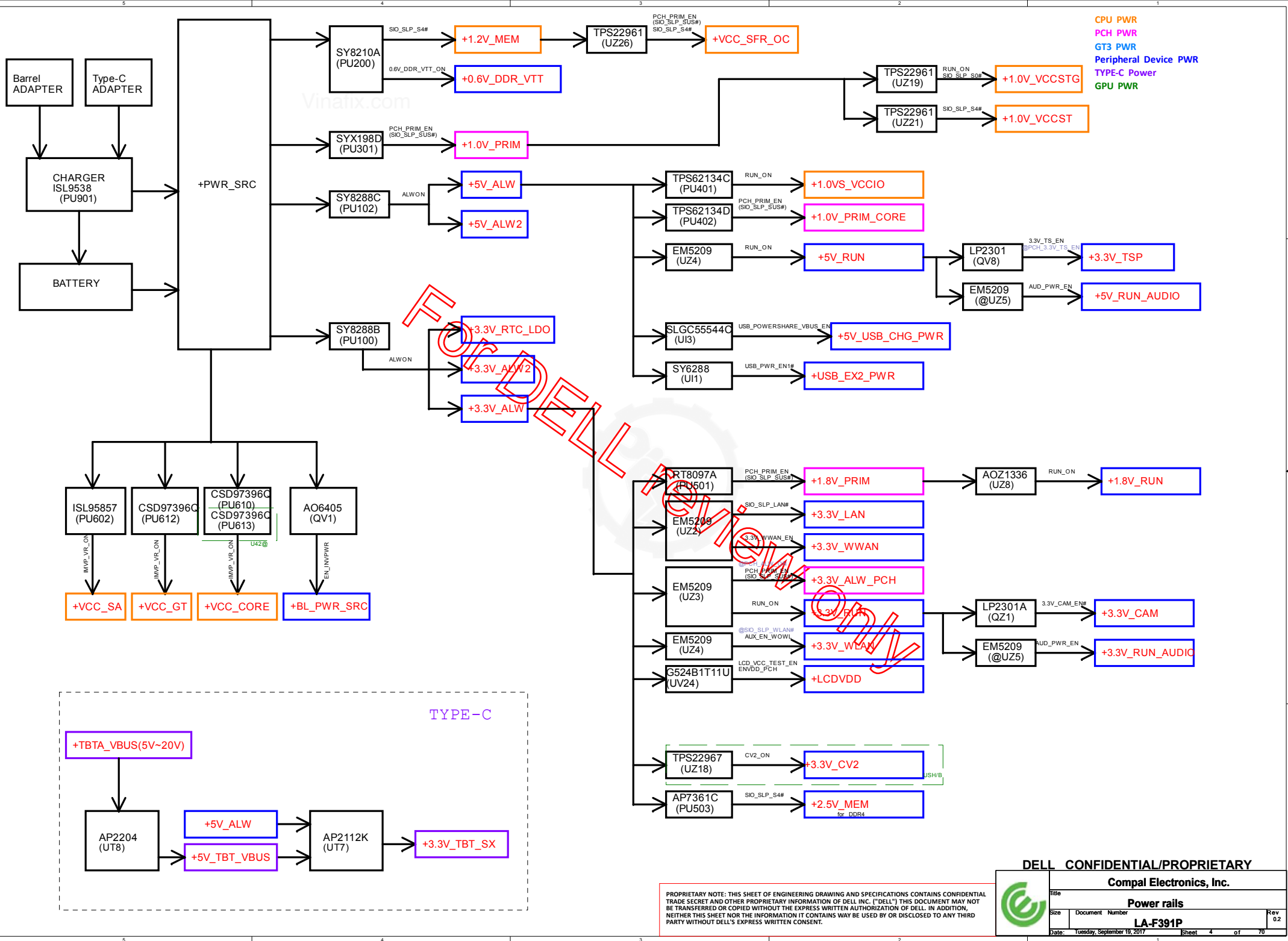
High Speed I/O (HSIO) Lane Multiplexing in KBL U

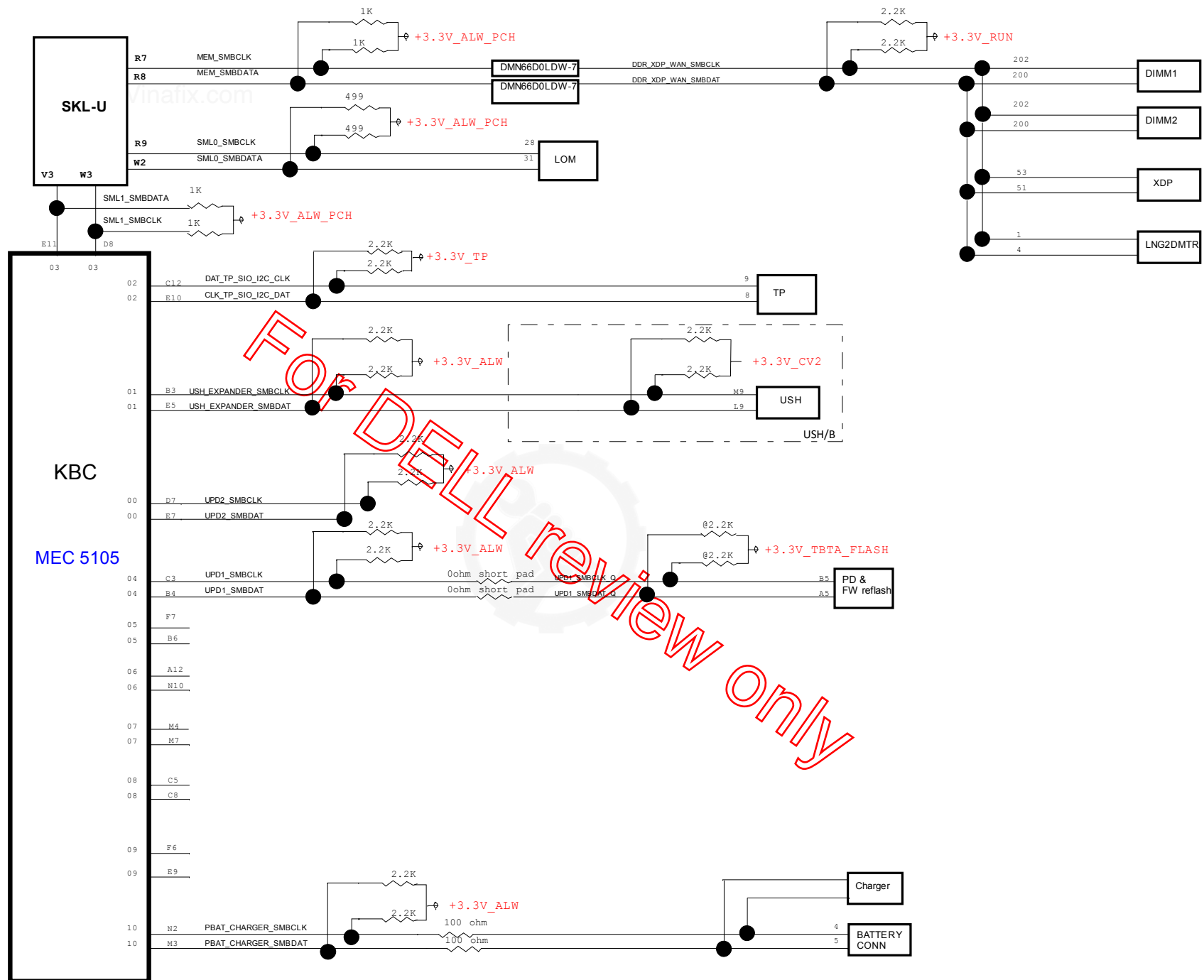


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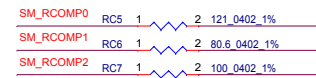
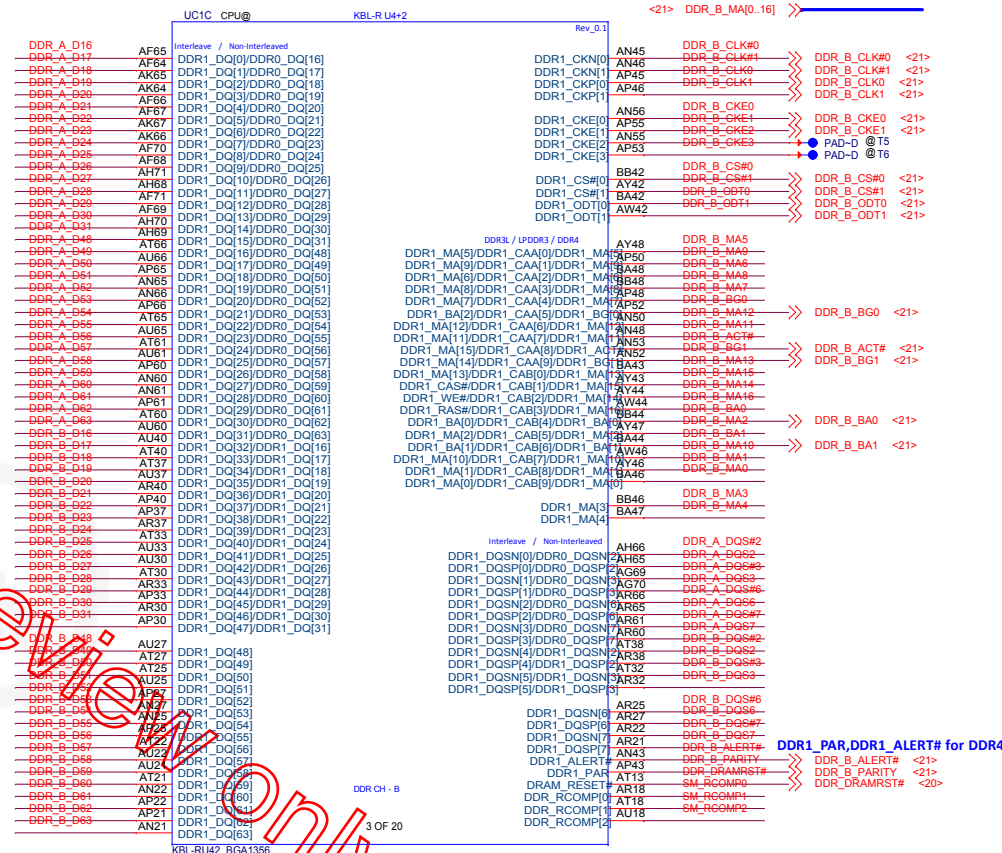
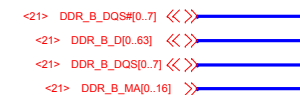
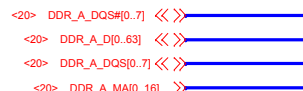




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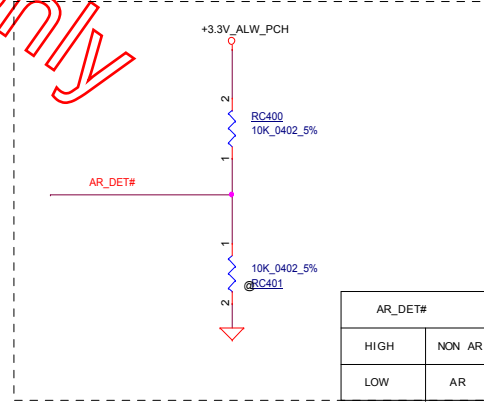
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

**CPU (2/14)**

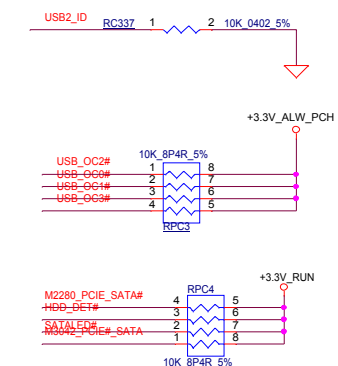
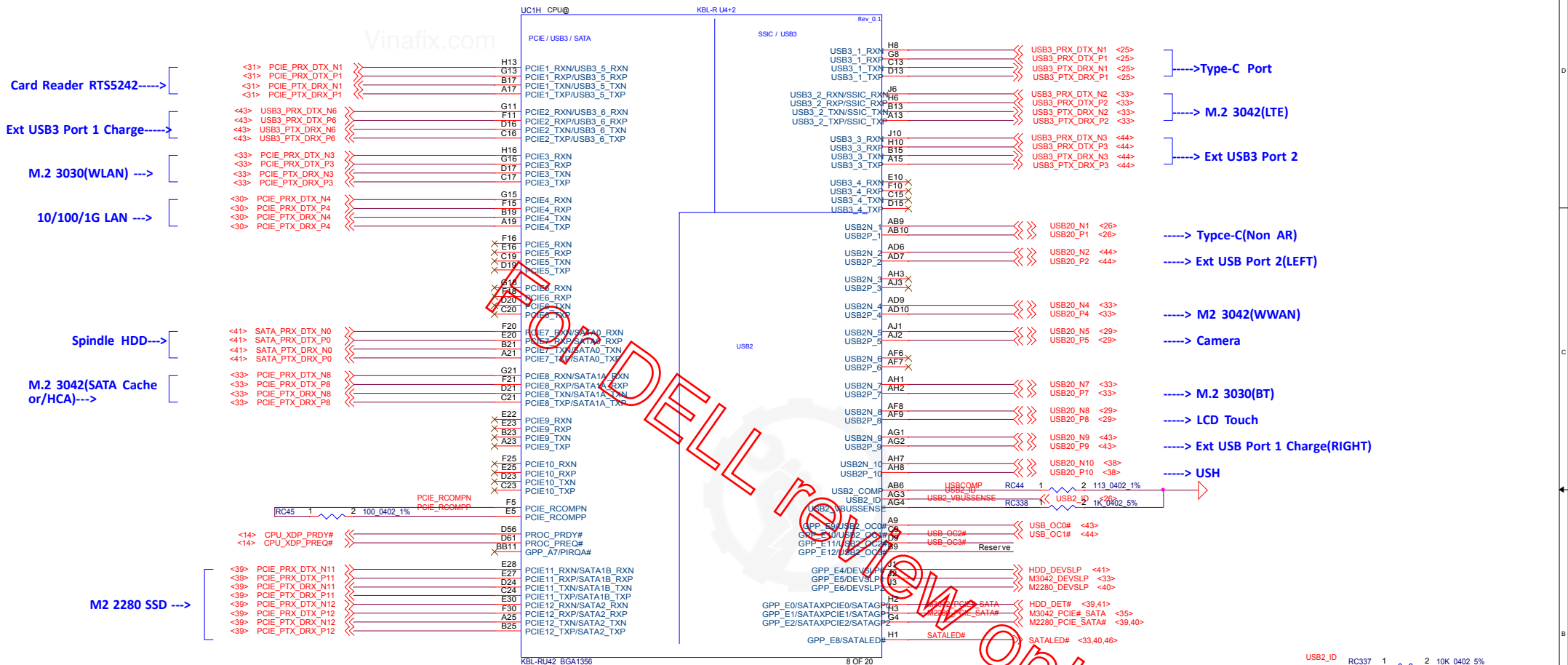
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RC349	
POP	China TPM
DEPOP	TPM

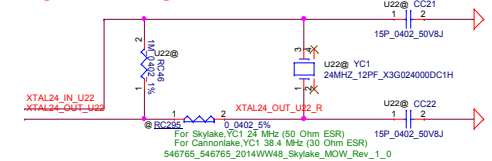


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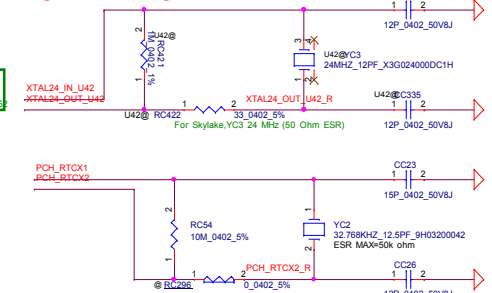
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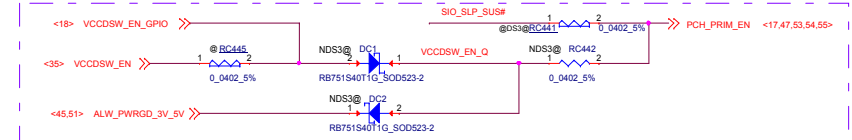
For KBL-R U22



For KBL-R U42



CMOS1 must take care short & touch risk on layout placement

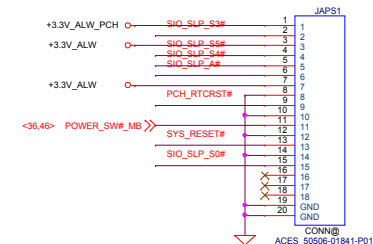
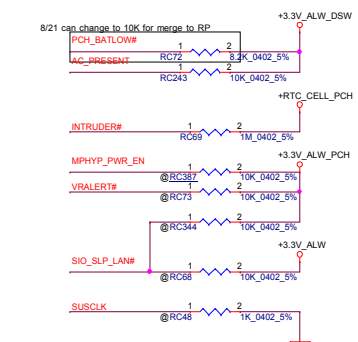


	RC439	RC440	RC441	RC442
Support DS3	V	X	X	V
No Support DS3	X	V	X	V

'V' mean POP,

'X' mean DE-POP

connect to VCCMPHYGTACON_1P0 enable pin



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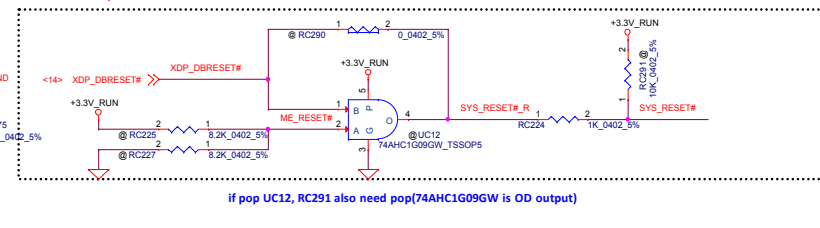
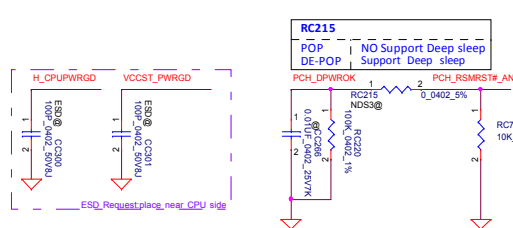
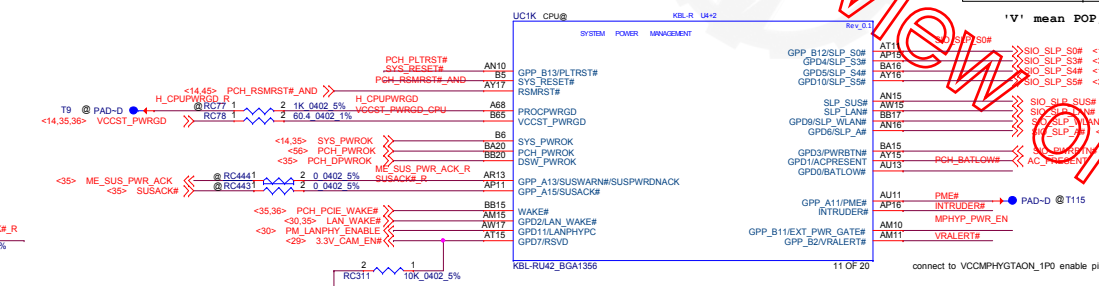
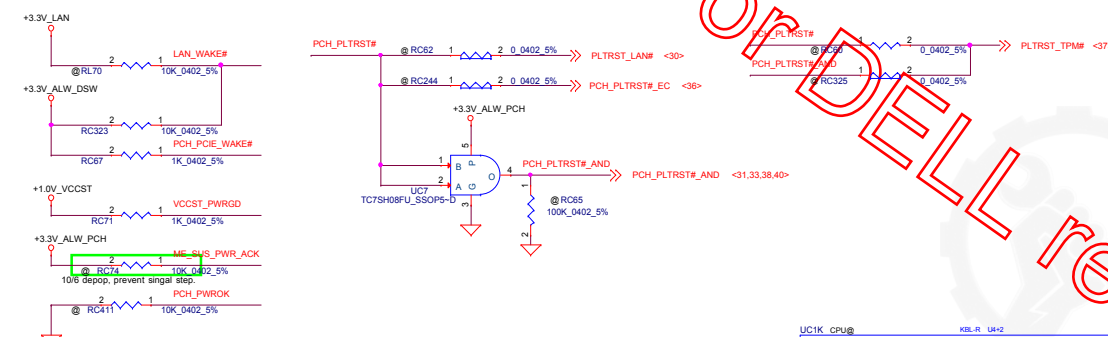
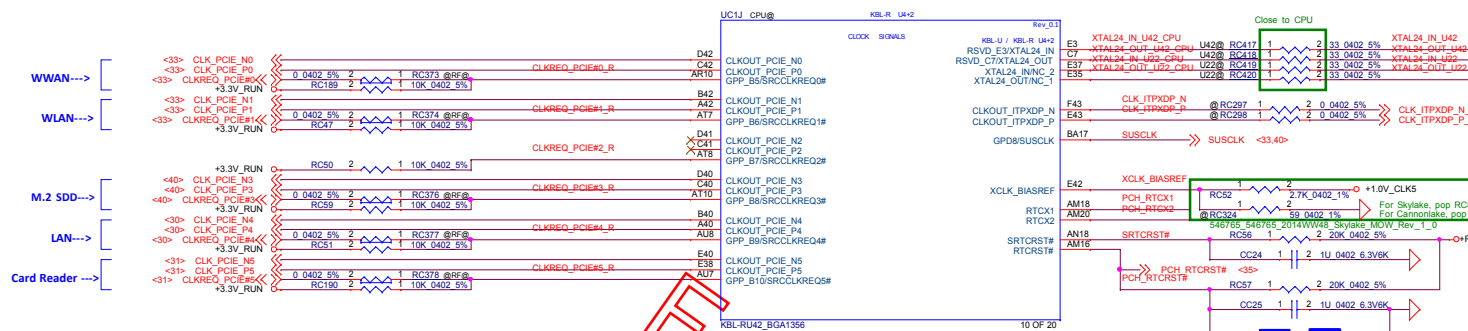
CPU (6/14)

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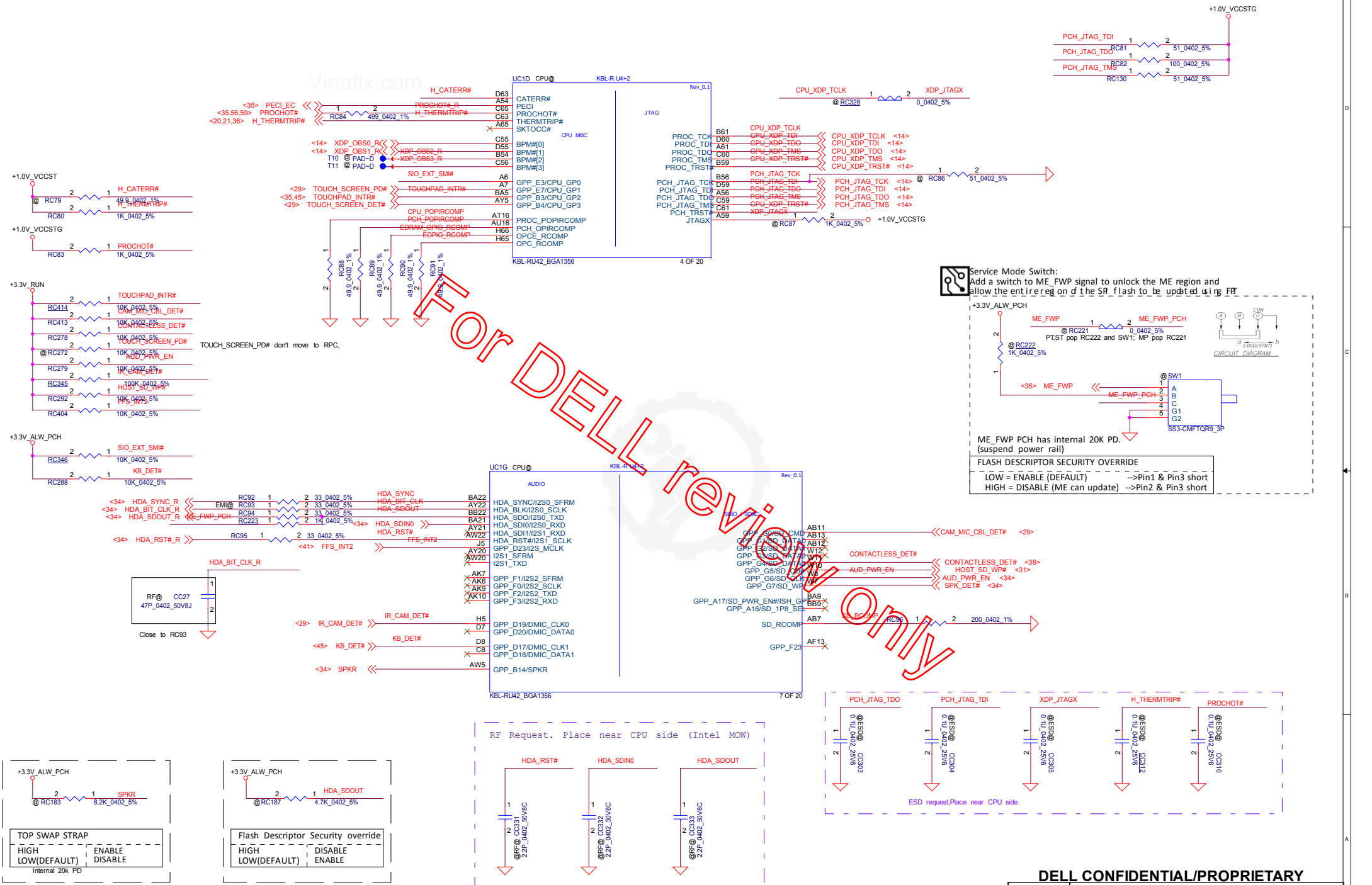
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Vinafix.com



if pop UC12, RC291 also need pop (74AHC1G09GW is OD output)

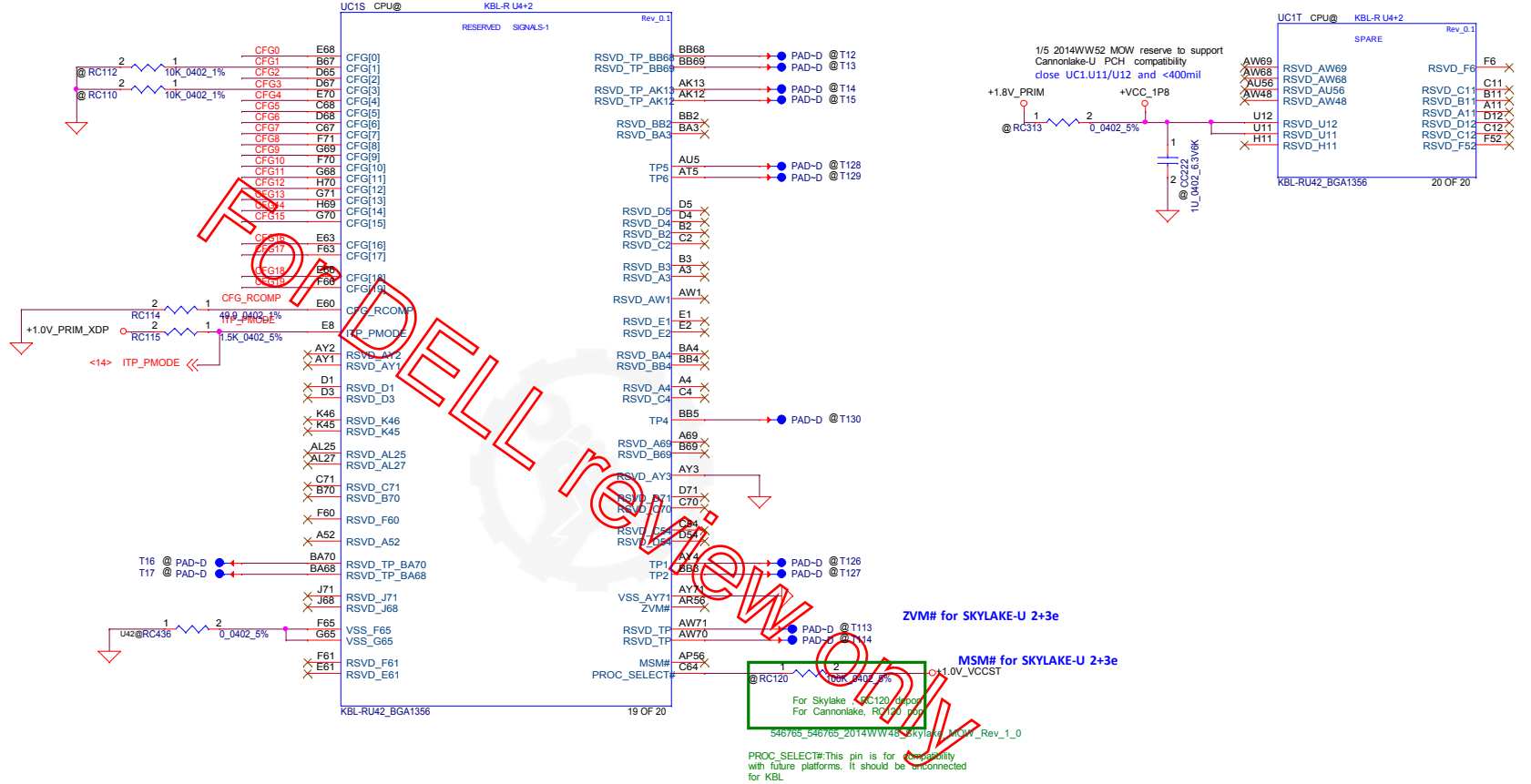
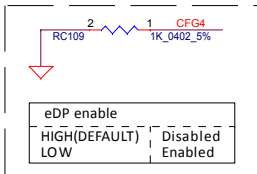
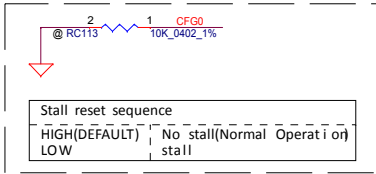


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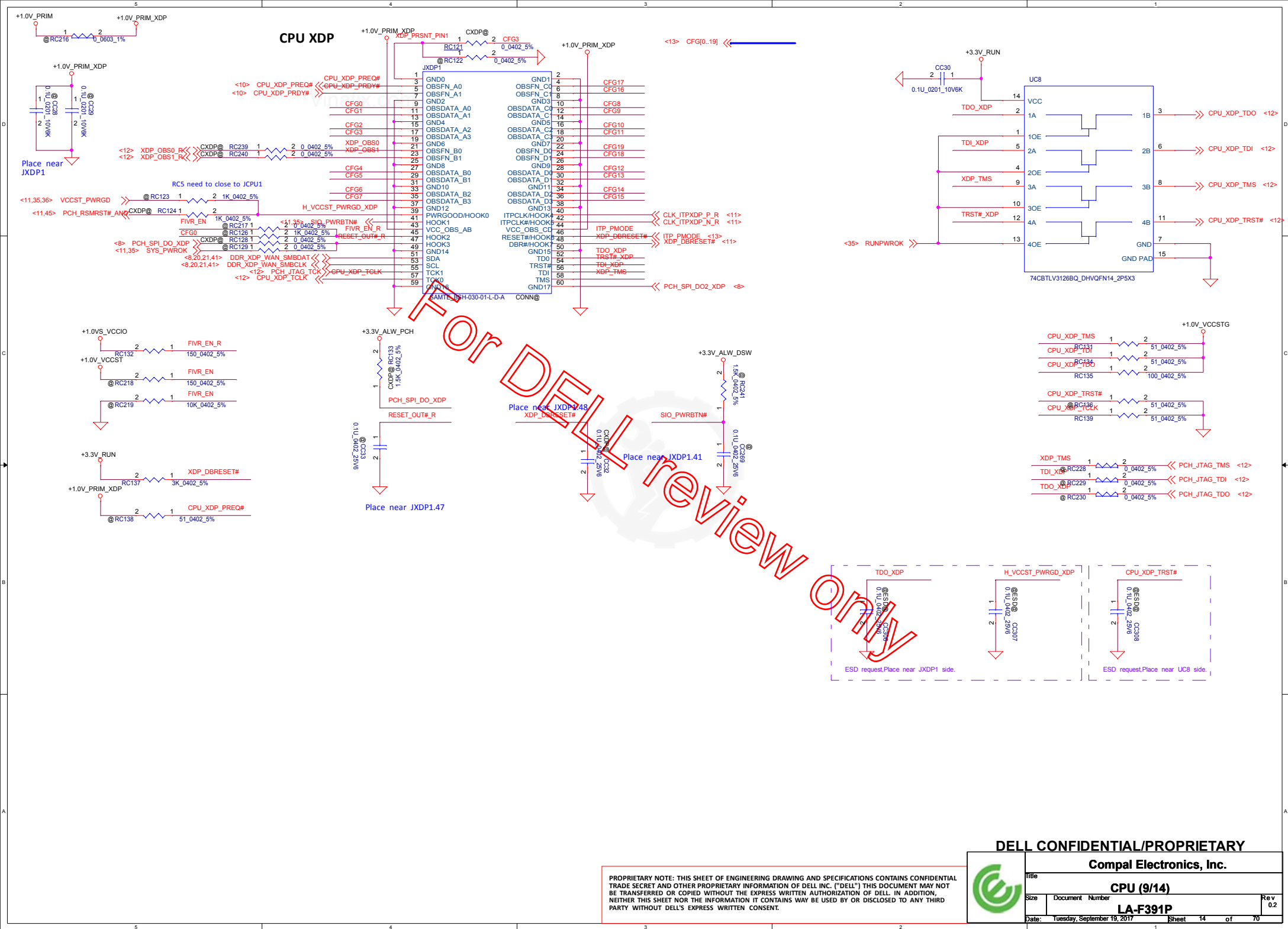
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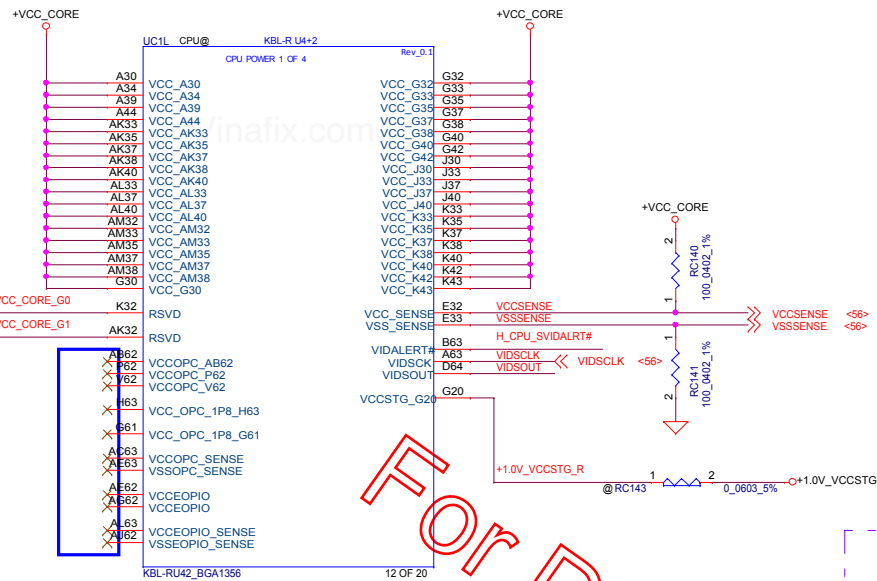
CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



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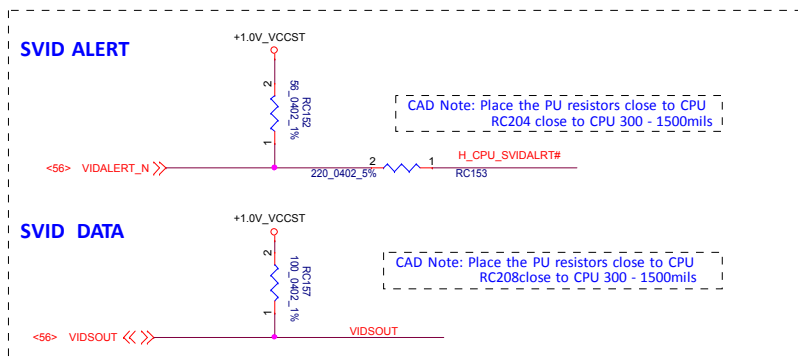
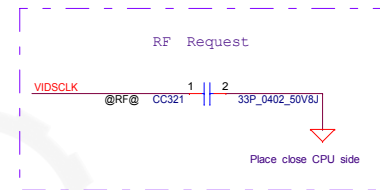
+VCC_CORE: 0.3~1.35V



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source



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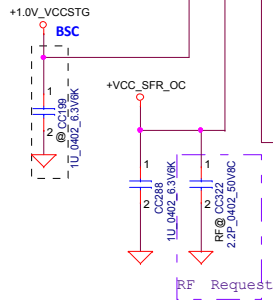
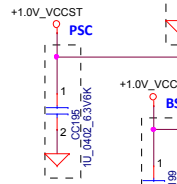
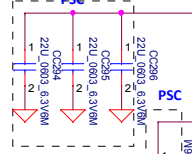
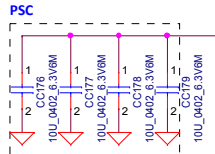


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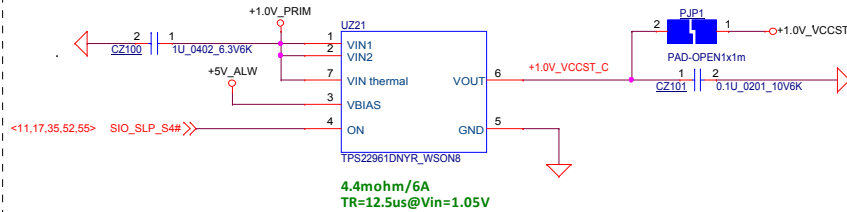
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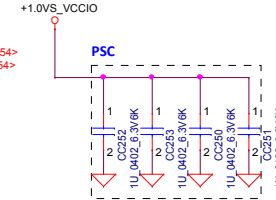
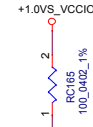
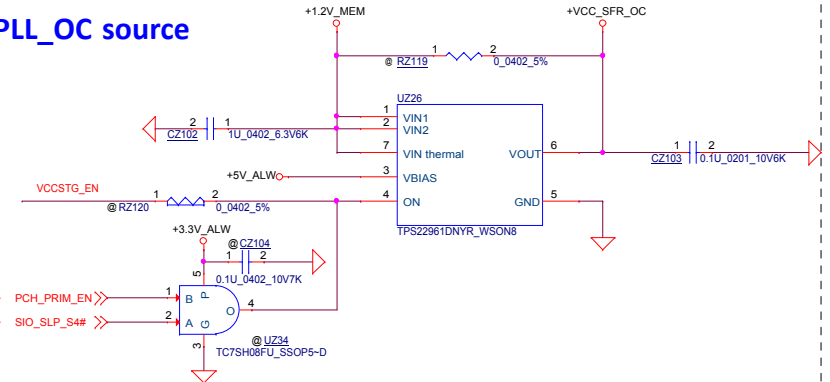
+1.2V_MEM_CPUCCLK
@RC231 1 2 0.0402_5%
VDDQ: 8.45A



+1.0V_VCCST source

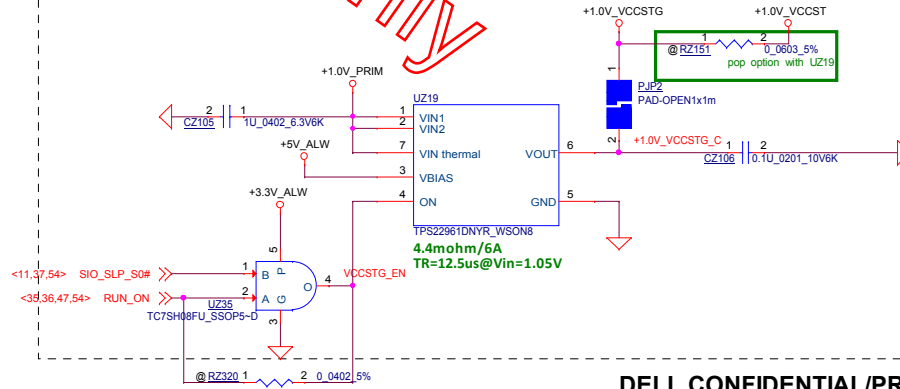


+VCCPLL_OC source



	S0	S0ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

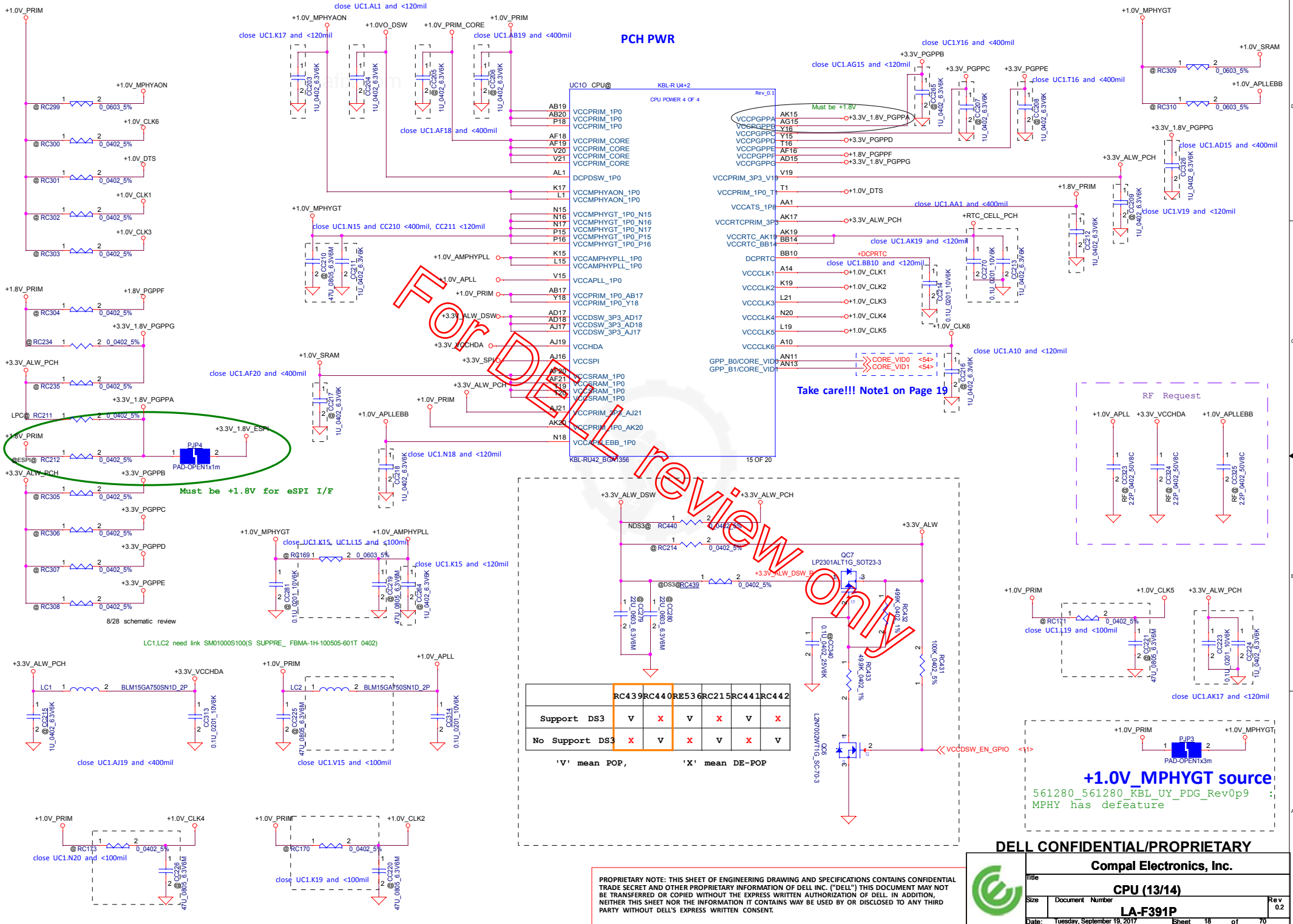
+1.0V_VCCSTG source



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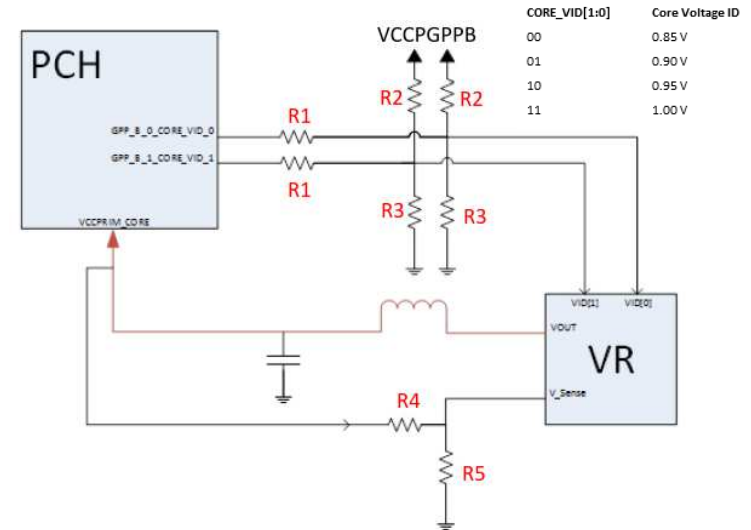
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Note1: VCCPRIM_CORE Implementat i on ū t h PCH CORE_V D Reco mnendati on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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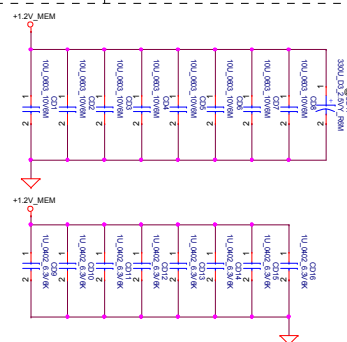


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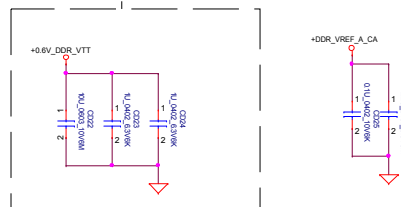
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```
<7> DDR_A_DQS[0..7] <<>>
<7> DDR_A_D[0..63] <<>>
<7> DDR_A_DQS[0..7] <<>>
<7> DDR_A_MA[0..16] >>>>
```

Layout Note:
Place near JDIMM1

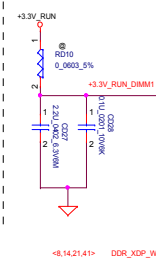


Layout Note:
Place near
JDIMM1.258

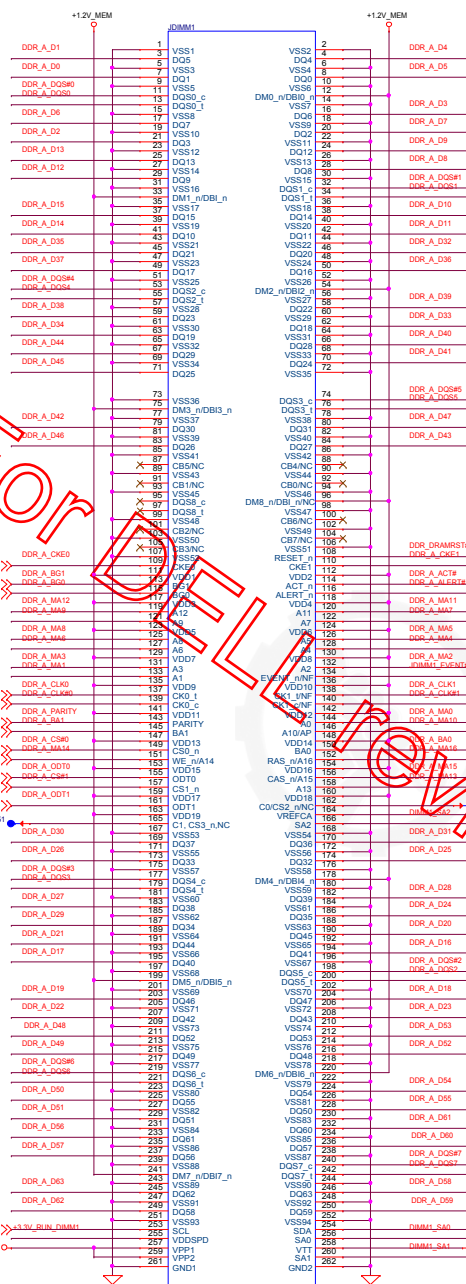


DIMM Select

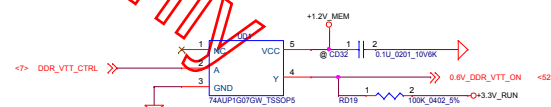
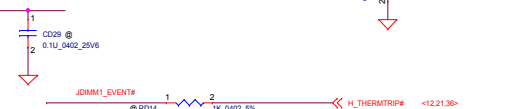
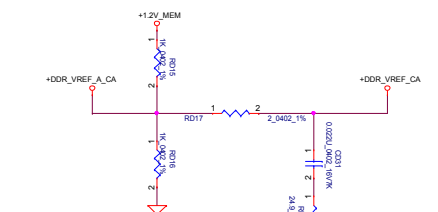
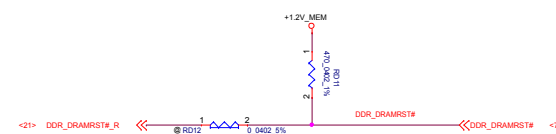
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



<8,14,21,41> DDR_XDP

[illegible]

LCN_DAN05-Q0406-0103
CONN@
LINK DAN05-Q0406-0103 DONE

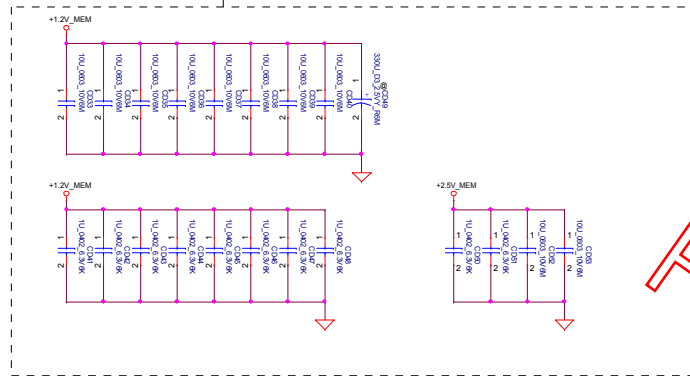


6/8 Change to SA00007WE00 DII

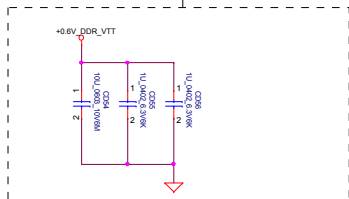
<7> DDR_B_DQS[0..7] <<>
 <7> DDR_B_DQ[0..63] <<>
 <7> DDR_B_DQS[0..7] <<>
 <7> DDR_B_MA[0..16] <<>

Layout Note:
Place near JDIMM2

Vinafix.com

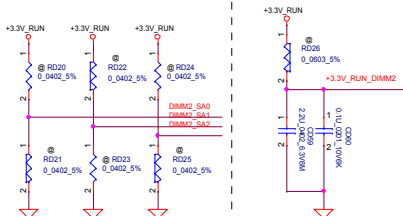


Layout Note:
Place near
JDIMM2.258



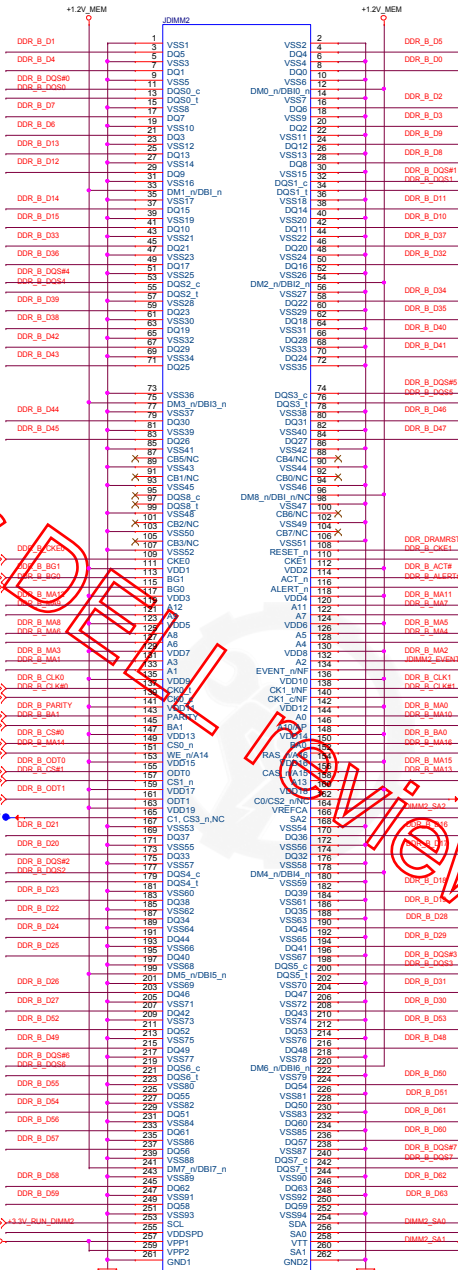
DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



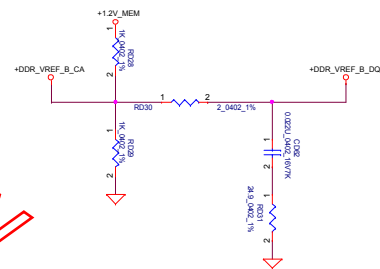
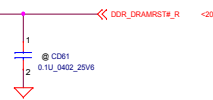
<8.14.20.41> DDR_XDP_WAN_SMBCLK

+2.5V_MEM



LINK DAN05-Q0406-0103 DONE

JDIMM2_EVENT# 1 2 1K_0402_5% << H_THERMTRIP# <12.20.36>



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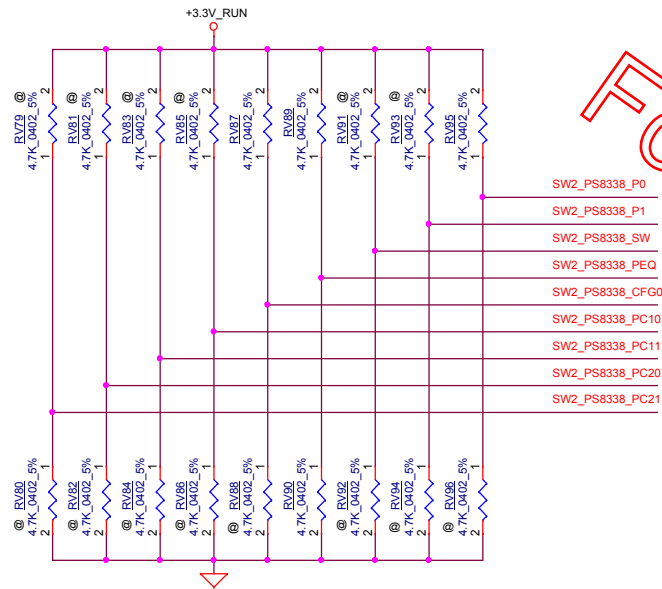
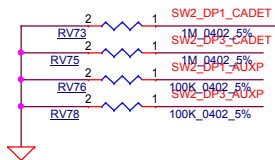
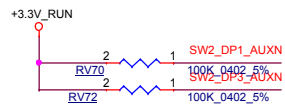
Compal Electronics, Inc.

DDR4

LA-F391P

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```
Port switching control or priority configuration. Internal pull down ~150KΩ,  
3.3V I/O  
For Control Switching Mode (CFG0 = L):  
SW = L: Port1 is selected (default)  
SW = H: Port2 is selected  
For Automatic Switching Mode (CFG0 = H):  
SW = L: Port1 has higher priority when both ports are plugged  
SW = H: Port2 has higher priority when both ports are plugged (default)
```

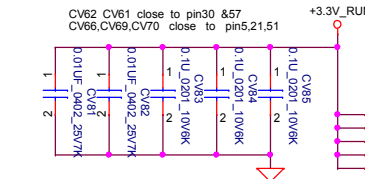
vender suggest MUX use LLEQ PEQ=M and P10=H !!

```

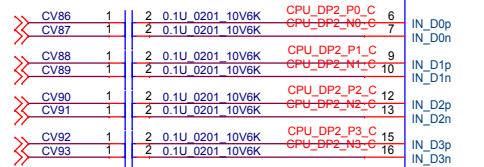
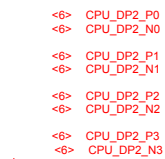
Programmable input equalization levels, Internal pull down at ~150Kohm, 3.3V I/O
PEQ =
L: default, LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M: LLEQ, compensate channel loss up to 8.5dB @HBR2

```

PIO:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
 PIO = L: Automatic EQ enable(default)
 H: Automatic EQ disable

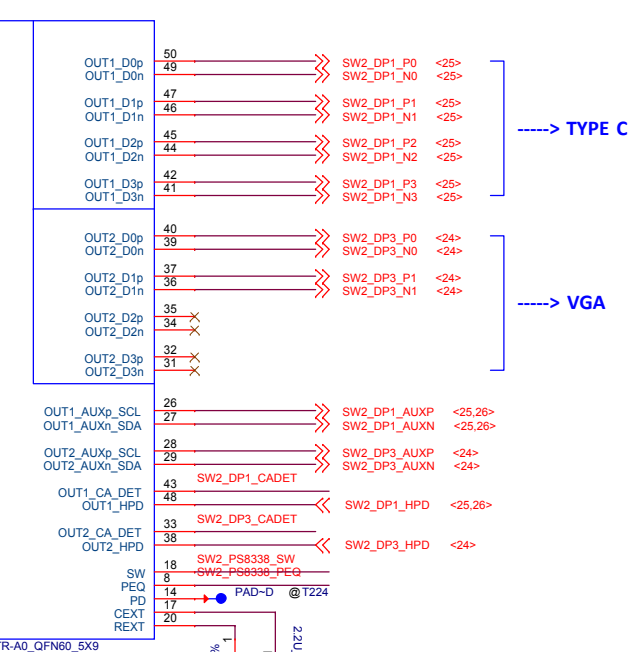
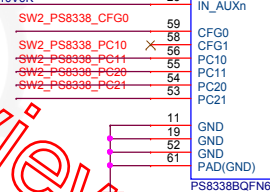


Priority: Type-C -> VGA



<6> CPU_DP2_HPD

for support TMDs signal need contact SCL/SDA to P22,23



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DP SW2 PS8348B

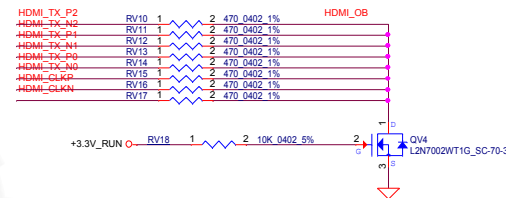
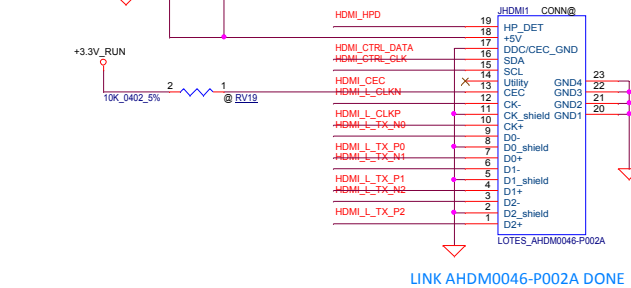
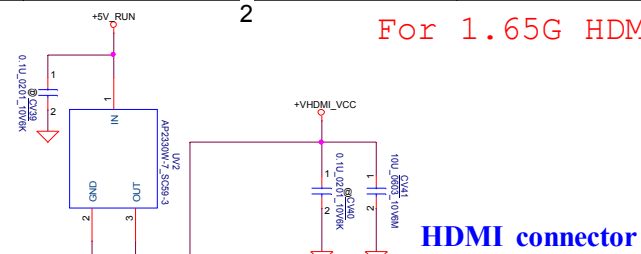
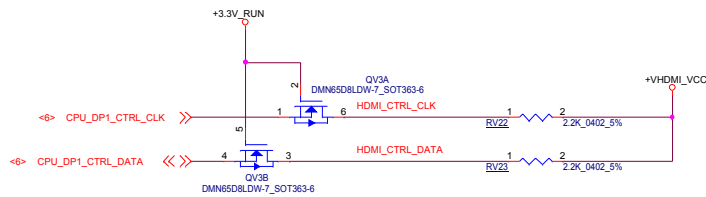
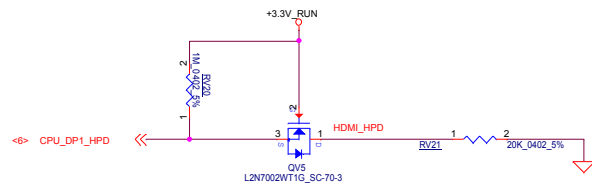
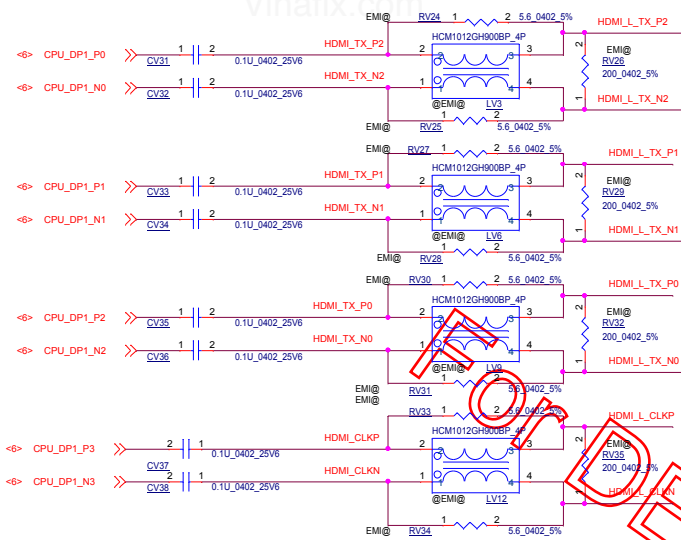
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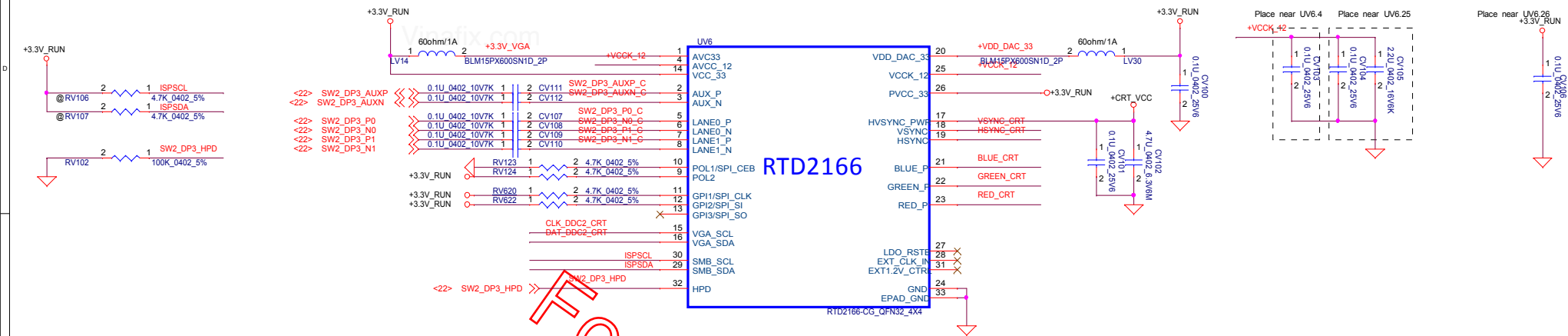




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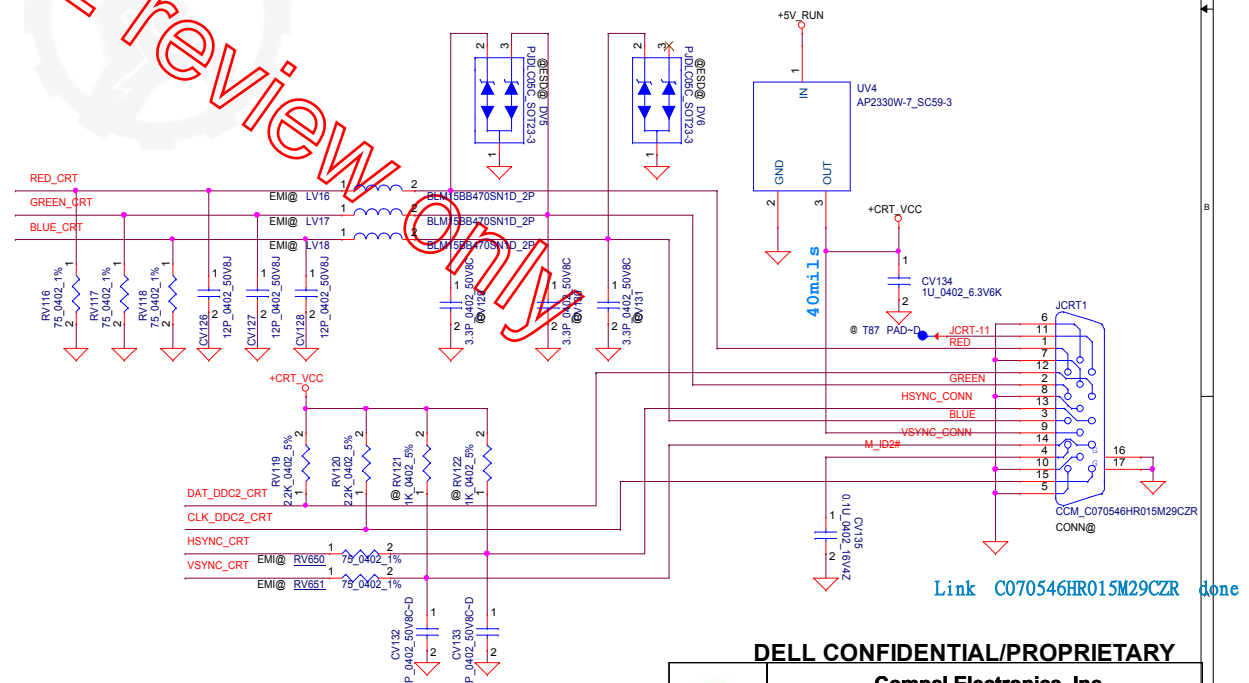
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Compal Electronics, Inc.			
Title		HDMI CONN	
Size	Document	Number	Rev
LA-F391P		02	
Date:	Tuesday, September 18, 2017	Sheet	23 of 70

For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



Link C070546HR015M29CZR done

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DP to VGA & VGA Conn

LA-F391P

0.2

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TUSB546: Pop RT300,Depop RT145,RT301
PS8743:Depop RT301,Pop RT145,RT300(change to 0.1uf)(VDD_DCI)

**DP/USB3 Repeater SW TUSB546**

LA-F391P

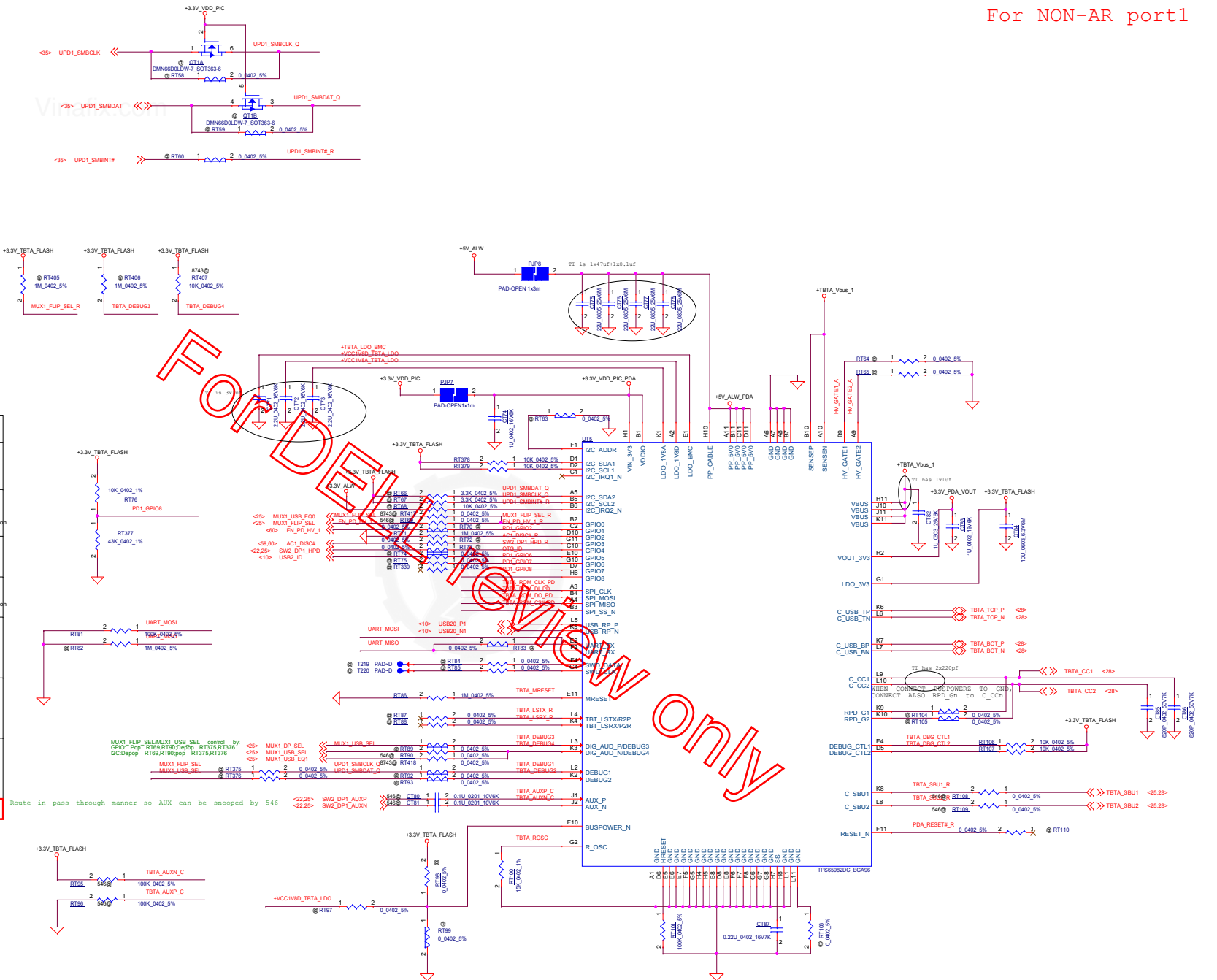
9

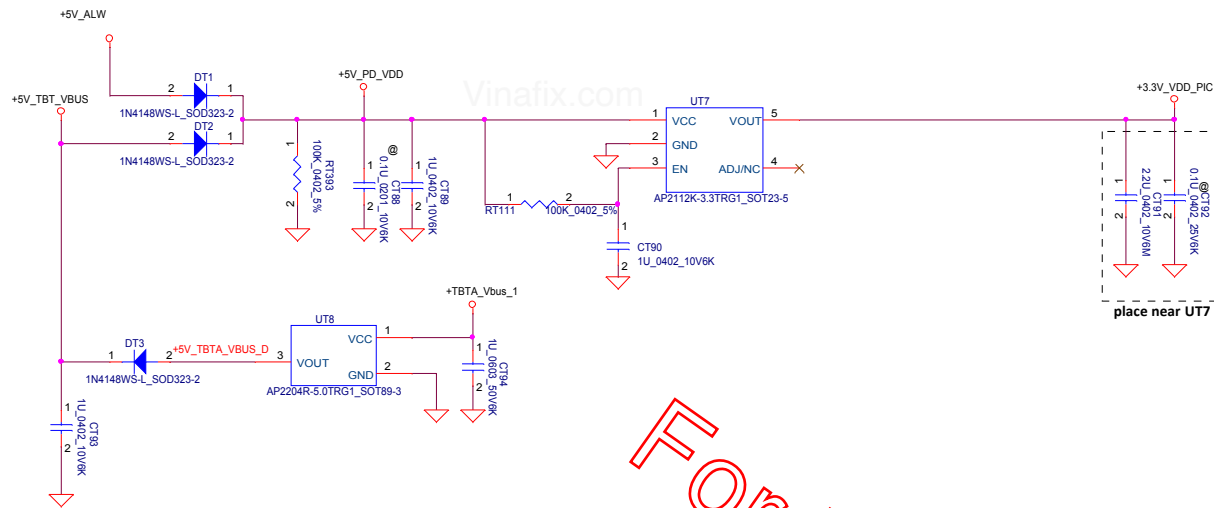
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Rev
0.2

Link TPS65982D (from SA00009W200 to SA00009W210) 08/04
running change from SA00009W210 to SA0000AK400 12/31

DIV = R2/(R1+R2)		Factory	Dense	Description
DIV_min	DIV_max	Configuration		
0.00	0.08	0	UFP only SV @0.9A Sink capability with "Ask for Max" for signaling from U3-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VDD supported	
0.10	0.18	1	UFP only SV @0.9A Sink capability with "Ask for Max" for signaling from U3-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations supported TI VDD supported	
0.20	0.28	2	UFP only SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VDD supported	
0.30	0.38	3	UFP only SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations supported TI VDD supported	
0.40	0.48	4	DRP SV @0.3-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VDD supported Accepts data and power role swaps, but does not initiate.	
0.50	0.58	5	DRP SV @0.3-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Source, C, D, and E pin configurations TI VDD supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.	
0.60	0.68	6	DRP SV @0.3-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Source, C, D, and E pin configurations TI VDD supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.	
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.	





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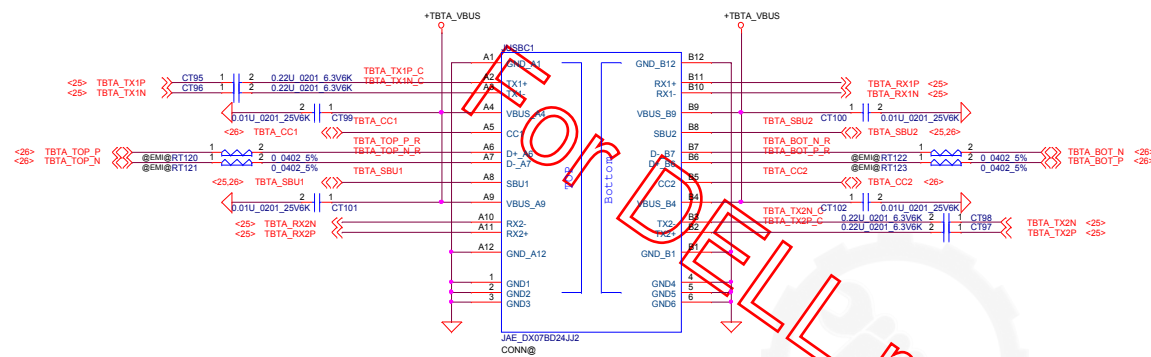
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Title			
[Type C]PD Power			
Size	Document Number	Rev	
	LA-F391P	0.2	
Date:	Tuesday, September 19, 2017	Sheet	27 of 70

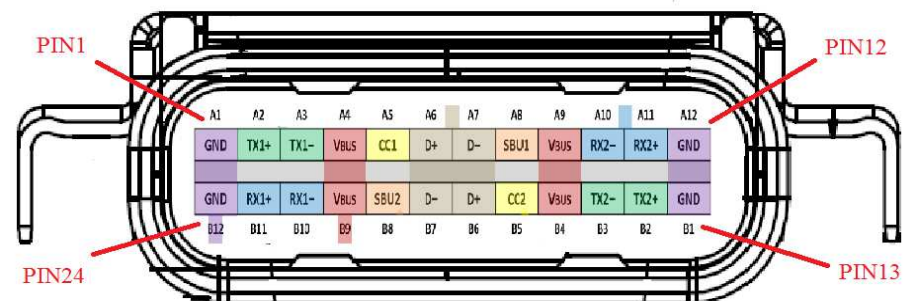
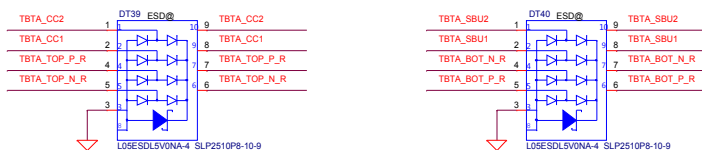
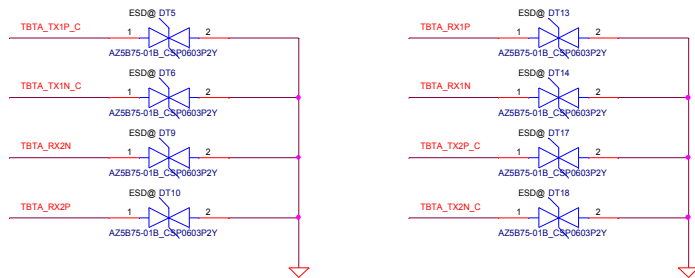
Vinafix.com



DX07BD24JJ2 LINK DONE

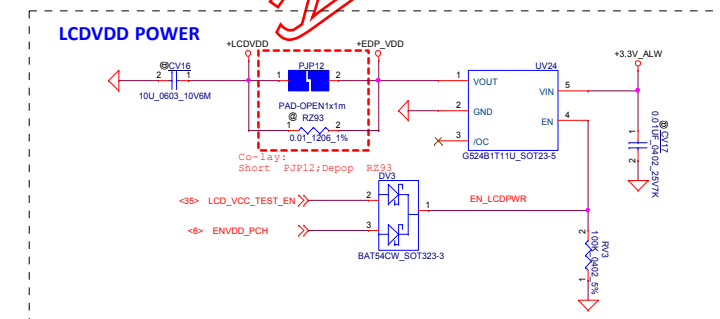
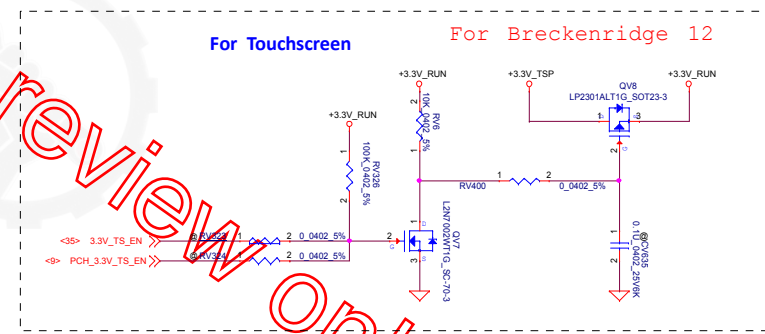
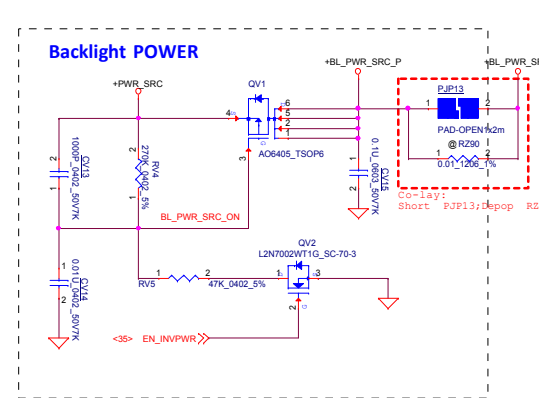
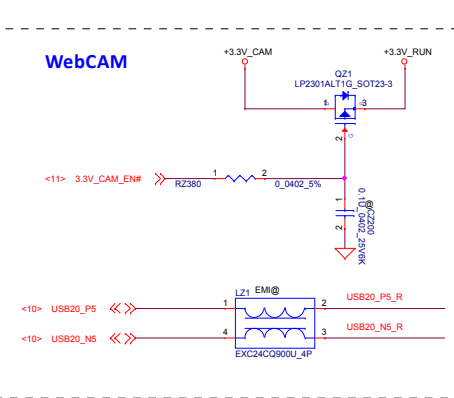
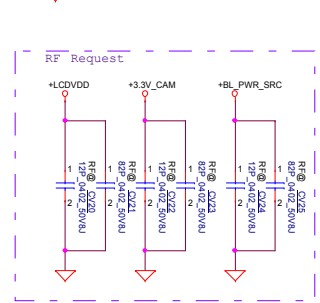
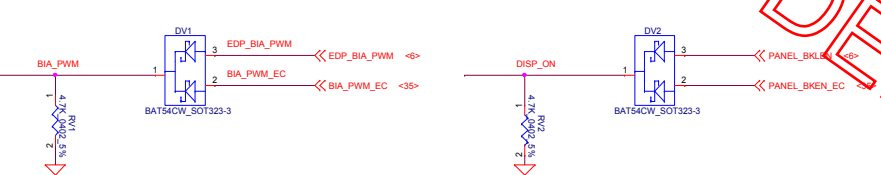
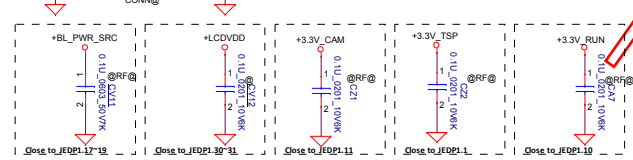
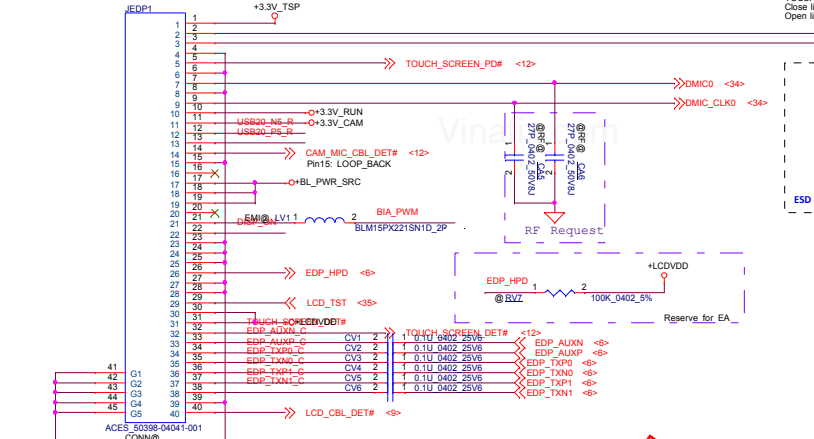
Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B

DT5, DT6, DT9, DT10, DT13, DT14, DT17, DT18,
change CPN from SC40000AT00 to SC40000DF00 06/07/2017



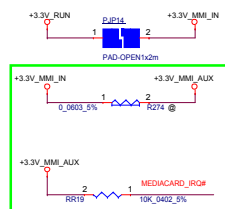
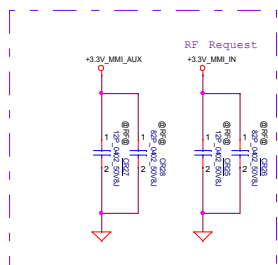
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LINK 50398-04041-001 DONE



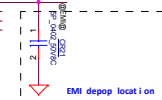
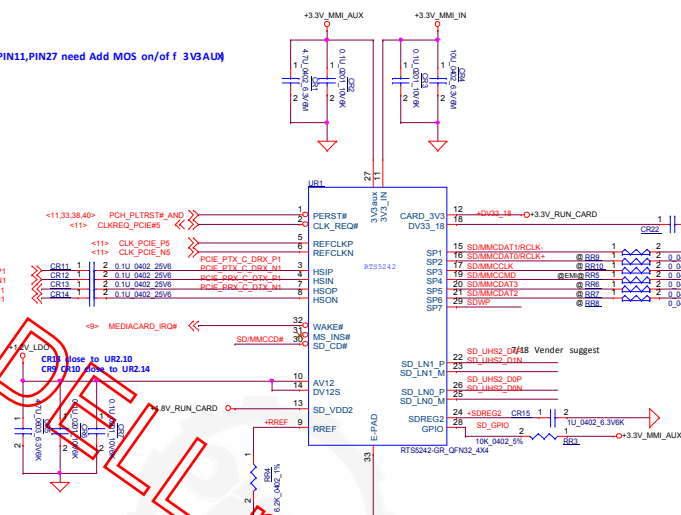
For 2LANE EDP & 3.3V_TSP
For Breckenridge & Steamboat 12

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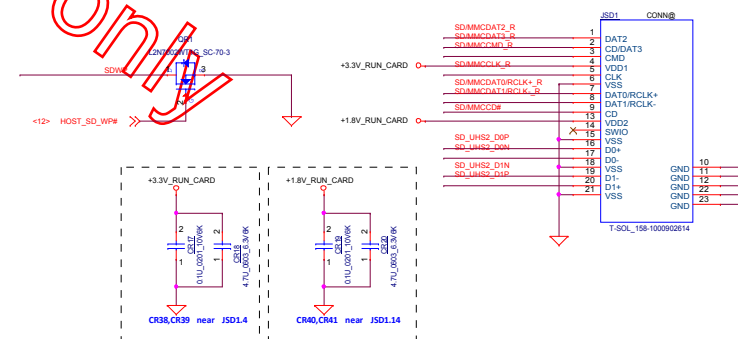


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

**Card Reader RTS5242**

LA-E391P

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E

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For NO SUPPORT
For DELL review only

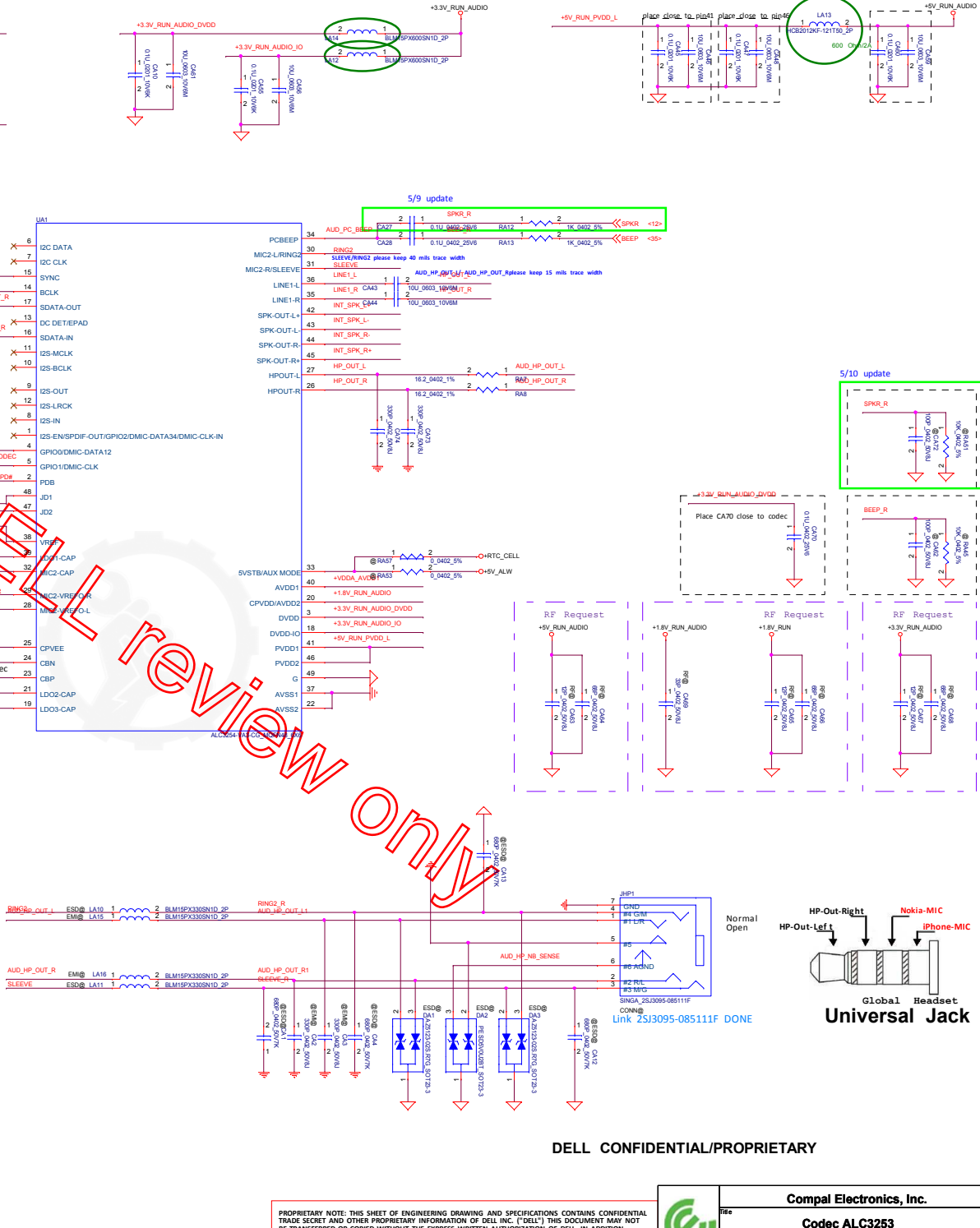
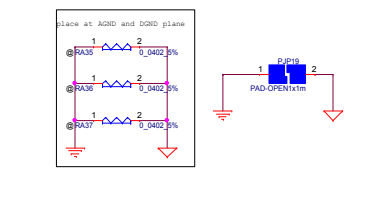
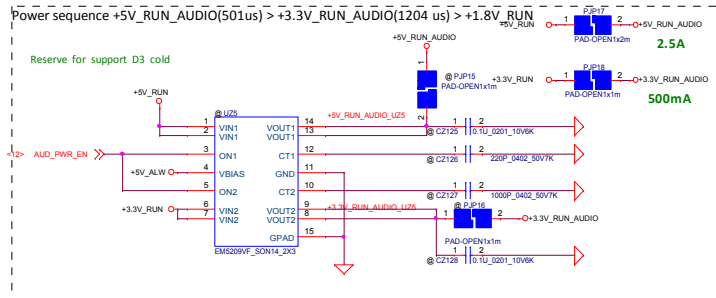
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Compal Electronics, Inc.



Title		PCIE REPEATER for M.2 3042		Rev
Doc	Document Number	LA-F391P		0.2
Date	Tuesday, September 18, 2017	Sheet	32	of 70

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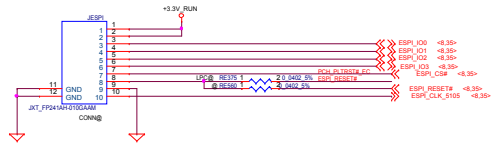
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6/8 Change to SA00007WE00 DII

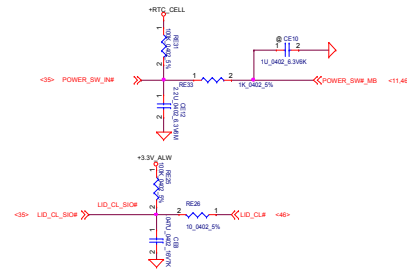
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PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

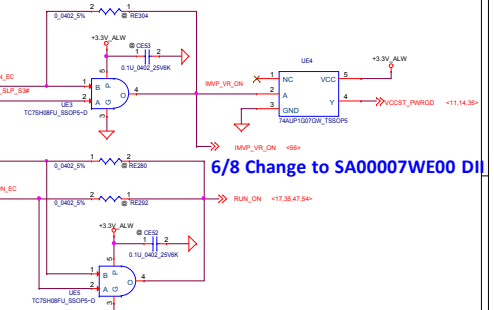
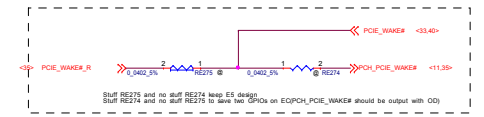


JXT_FP241AH-010GAAM LINK DONE

LPC @Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

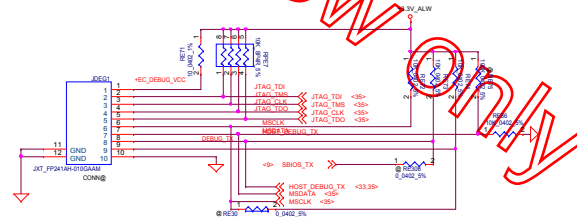


RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	.
1K	4700p	.

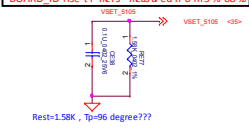


RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	.

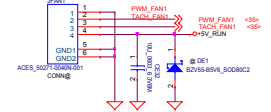
PD_ACE_DET# rise t1 me1s measured from 5% to 68% BOARD_ID rise t1 me1s measured from 5% to 68% SYSTEM_ID rise t1 me1s measured from 5% to 68%



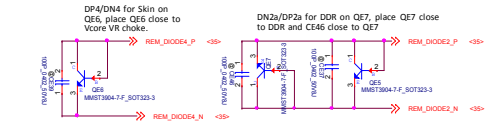
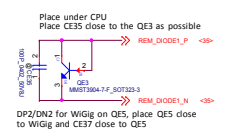
JXT_FP241AH-010GAAM LINK DONE



Link 50271-0040N-001 DONE



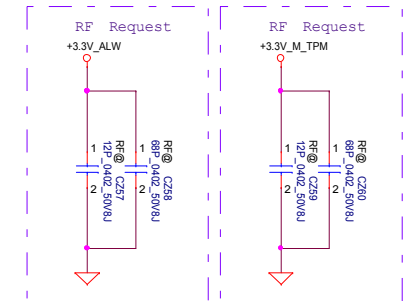
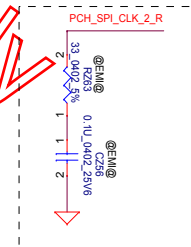
5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



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Doc	MECS105 Support
Doc	LA-F391P
Rev	1.0

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	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V _{RUN} Power VHIO - V _{SPI} Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V _{RUN} power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V _{SPI} power

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USH & TPM

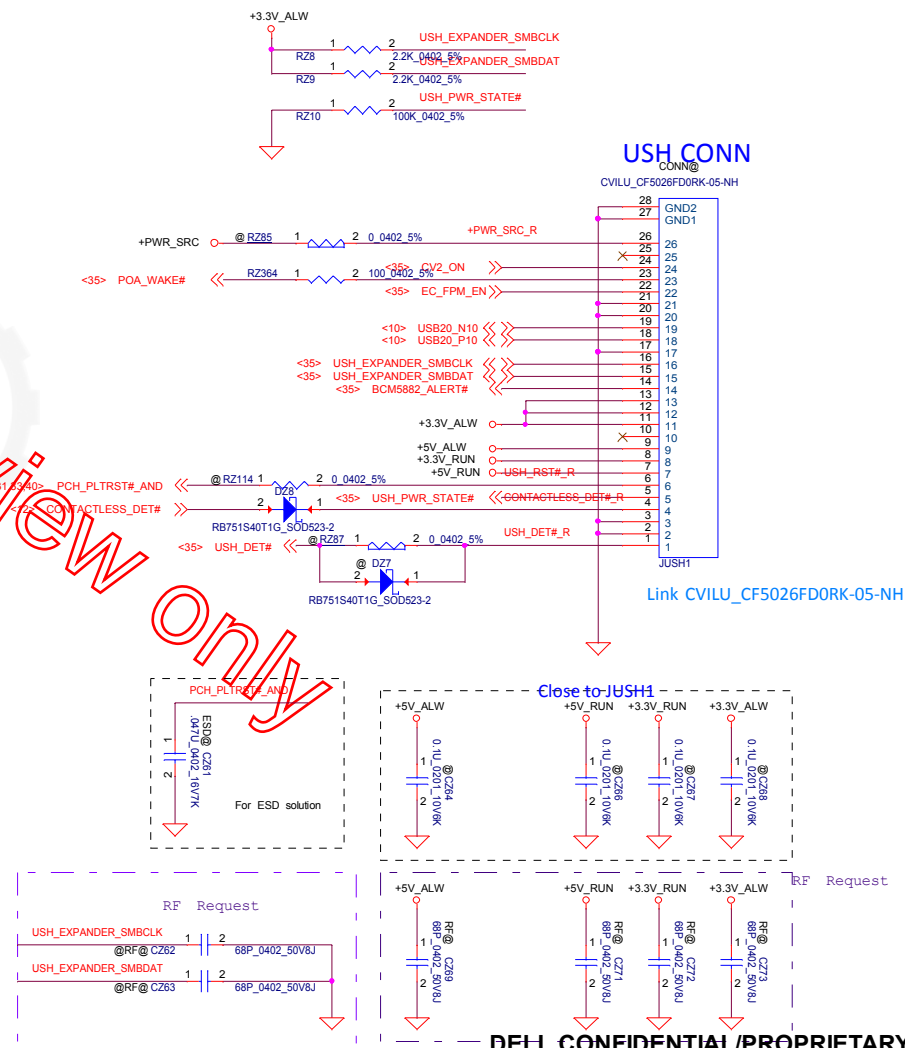
LA-F391P

Date: Tuesday, September 19, 2017

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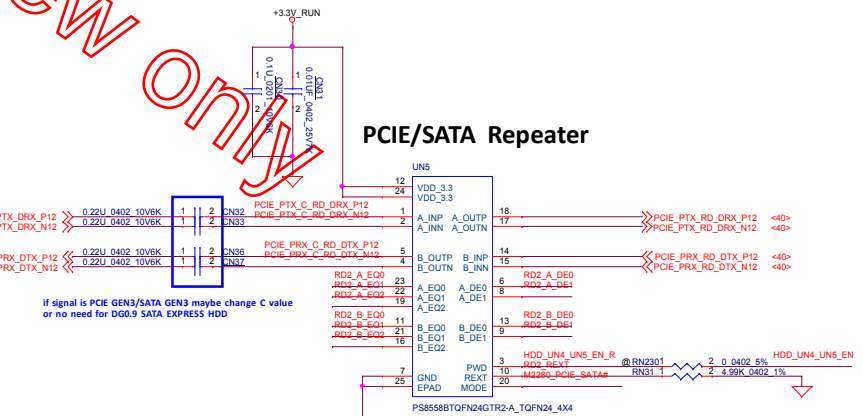
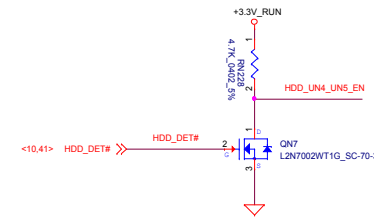
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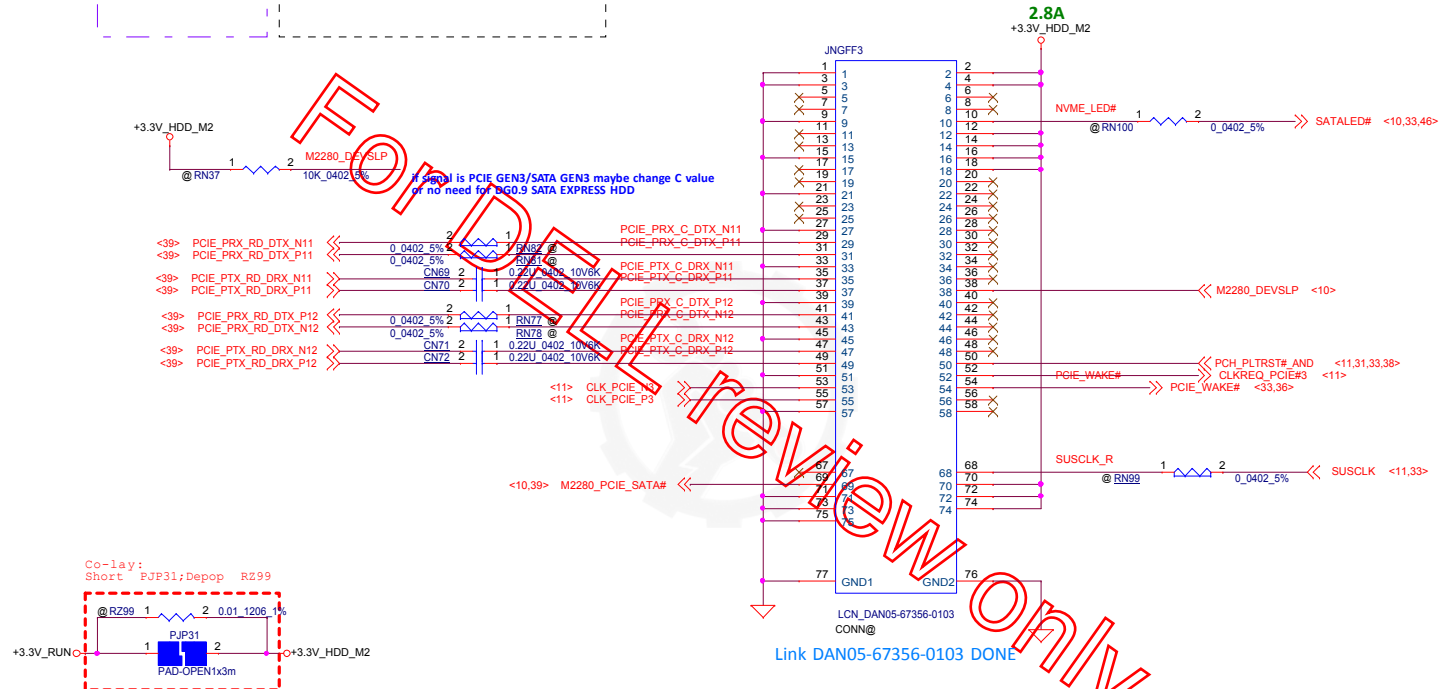
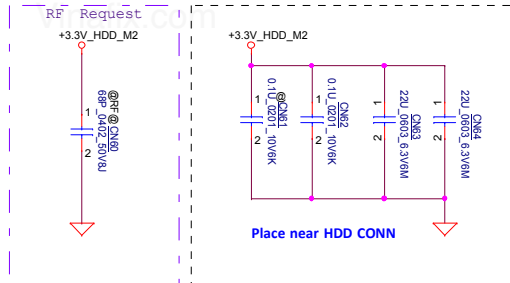
Compal Electronics, Inc.

Title			USH & TPM
Size	Document Number	Rev 0.2	
Date			LA-F391P
Tuesday, September 19, 2017			Sheet 38 of 70



Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

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M2 2280 Socket

LA-F391P

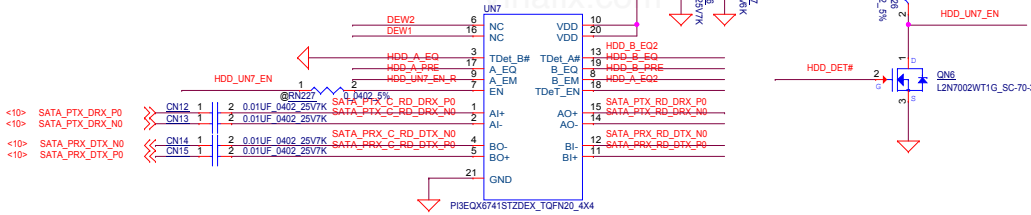
Date: Tuesday, September 19, 2017 Sheet 40 of 70

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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDet_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

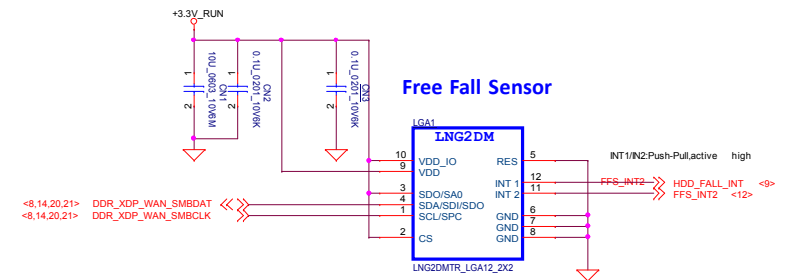
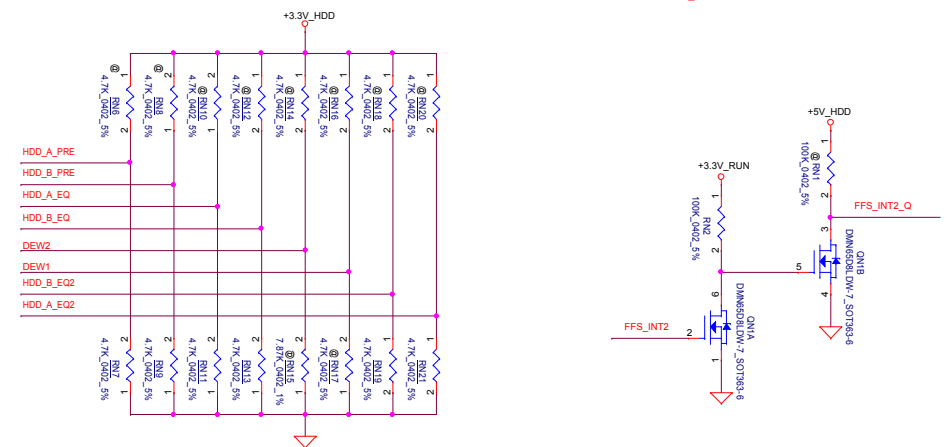
SATA Repeater



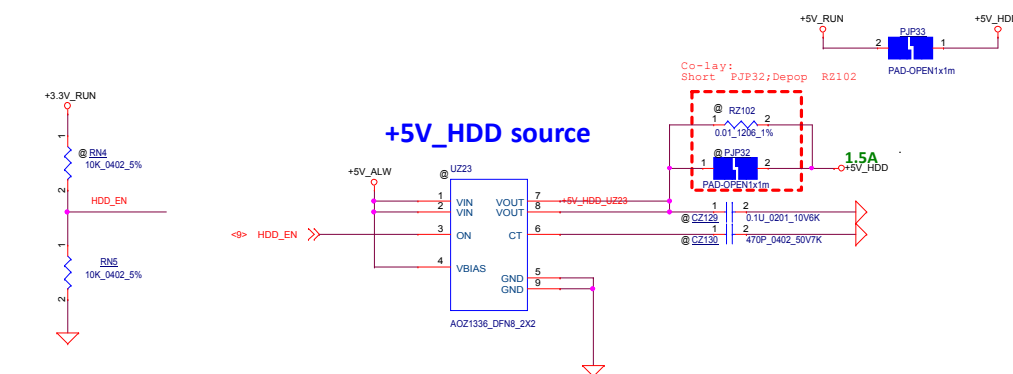
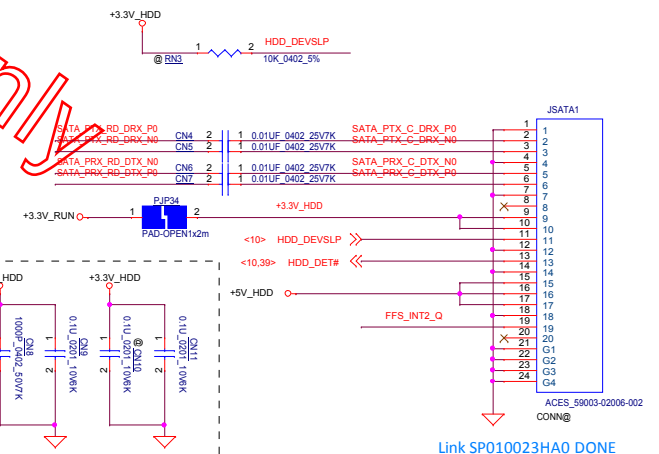
		HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom	PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN8)
TI	SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (I/P)	NC (I/P)	PH (RN6)	PH (RN8)
Parade	PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN5)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		1	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		1	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2	EQ1	A_EQ	B_EQ	A_EM	B_EM
		(M = VDD/2)					
		0	M	2.4dB	2.4dB		
		0	0	7.4dB	7.4dB		
		0	1	14.4dB	14.4dB	0	0dB
		M	M	12.2dB	12.2dB	M	-3.5dB
		M	0	9.4dB	9.4dB	1	-1.5dB
		M	1	13.3dB	13.3dB		
		1	M	6.2dB	6.2dB		
		1	0	11.2dB	11.2dB		
		1	1	5dB	5dB		

* red color is current setting



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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SATA Repeater&HDD CONN			
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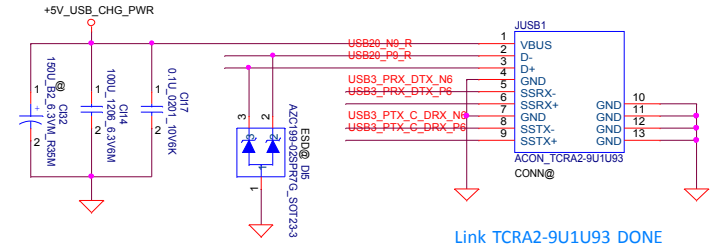
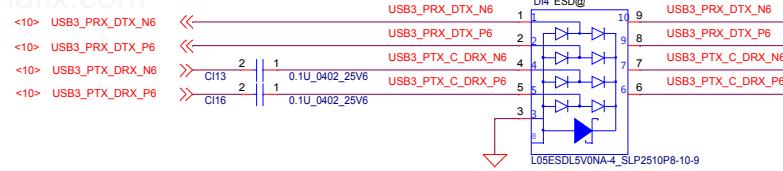


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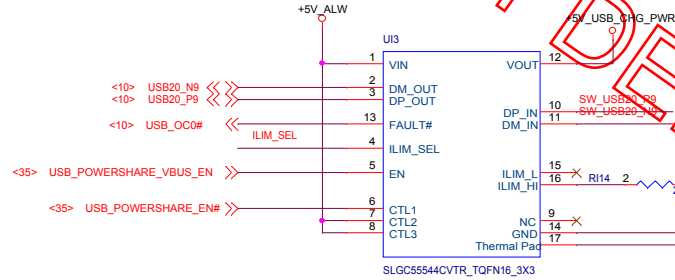
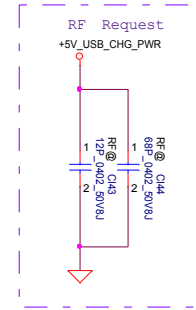
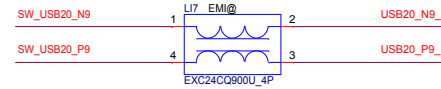
Title			USB3.0 Repeater	
Size	Document Number	LA-F391P		Rev 0.2
Date:	Tuesday, September 19, 2017	Sheet	42	of 70

For w/o Repeater

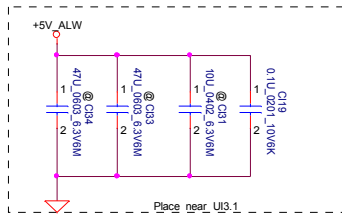
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Link TCRA2-9U1U93 DONE



Link Seligro SA000097E10 Done
MAIN:SLGC55544CVTR



Place near UI3.1

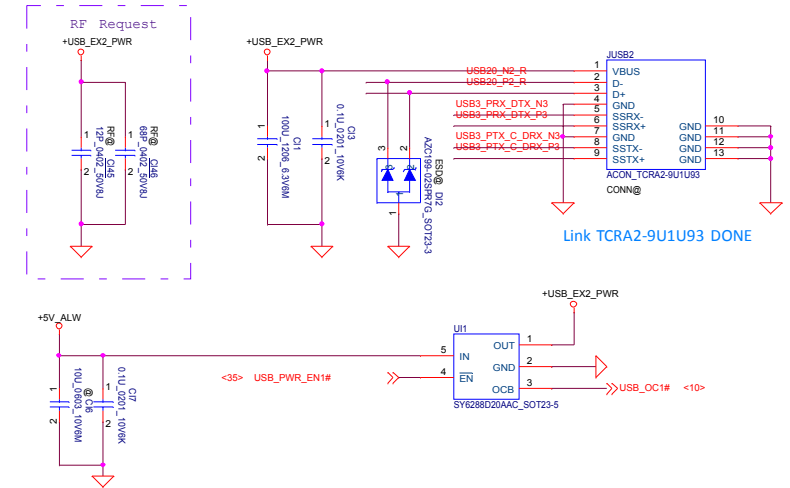
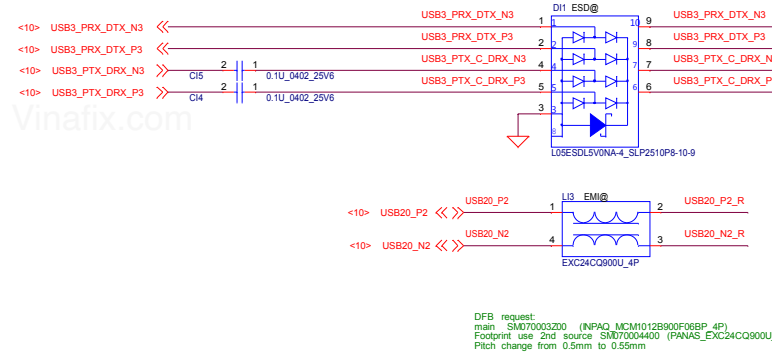
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Title			
JUSB1+PS			
Size	Document Number	Rev	
	LA-F391P	0.2	
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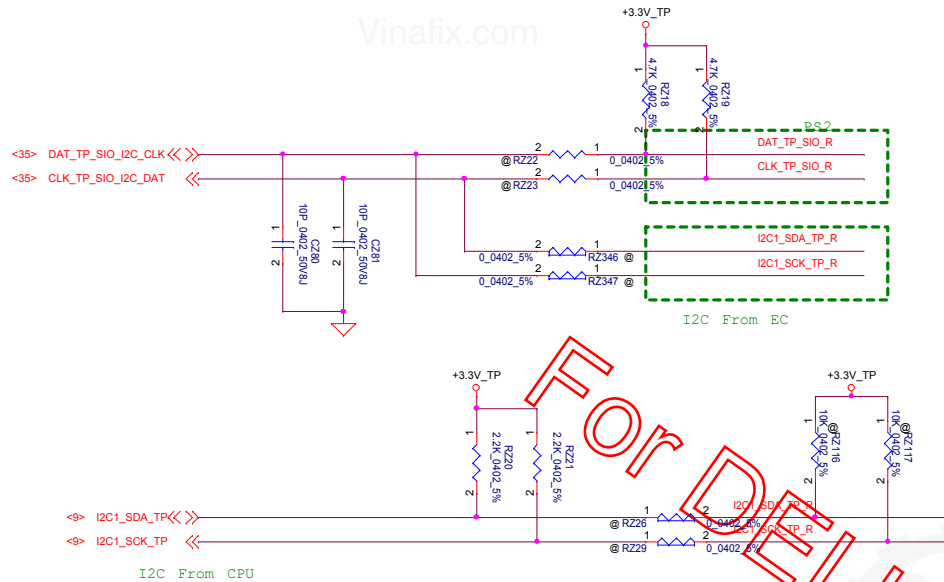
Compal Electronics, Inc.



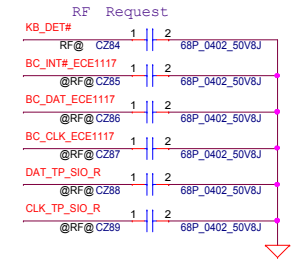
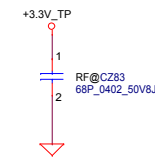
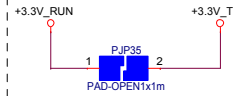
Computer Electronics, Inc.			
Title			
JUSB2			
Size	Document Number		Rev
	LA-F391P		0.2
Date:	Tuesday, September 19, 2017	Sheet 44 of 70	

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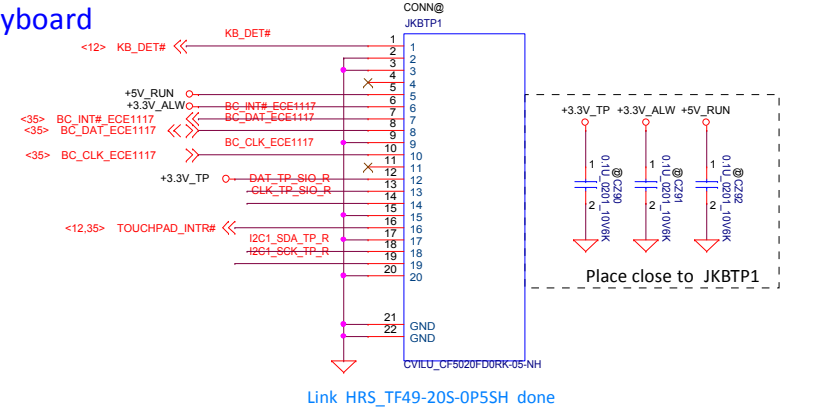
Touch Pad



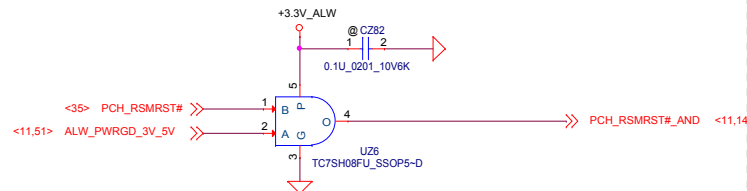
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



Keyboard



RSMRST circuit



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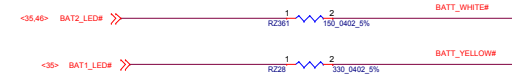
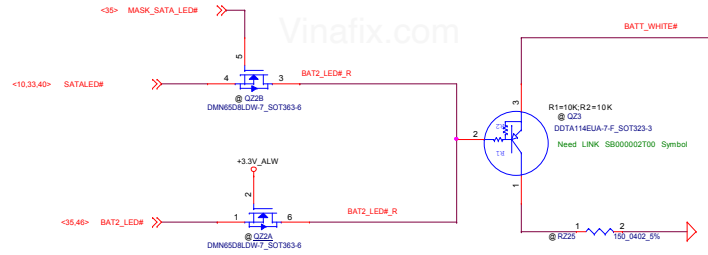


Title			
Keyboard			
Size	Document	Number	Rev
		LA-F391P	0.2
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Battery LED

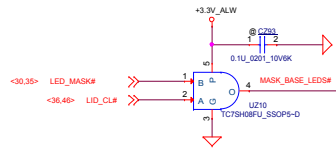
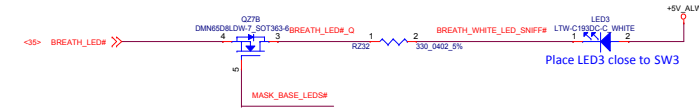
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key - Fn+F1

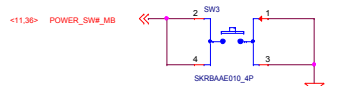


Breath LED

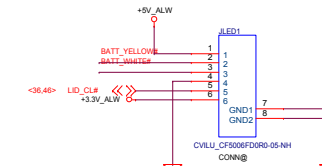
LED PIN change to SC50000FL00 from SC50000BA00



POWER & INSTANT ON SWITCH



LED board CONN

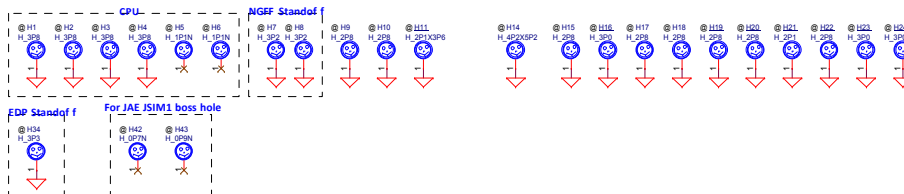


Fiducial Mark



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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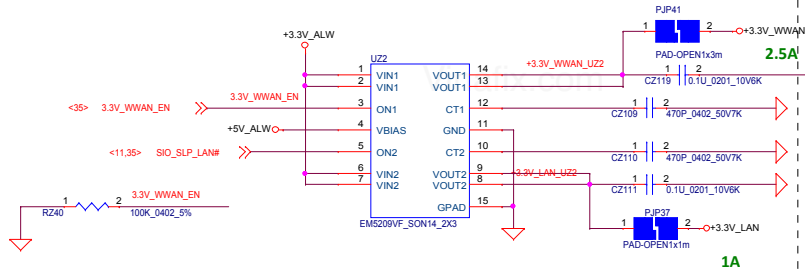
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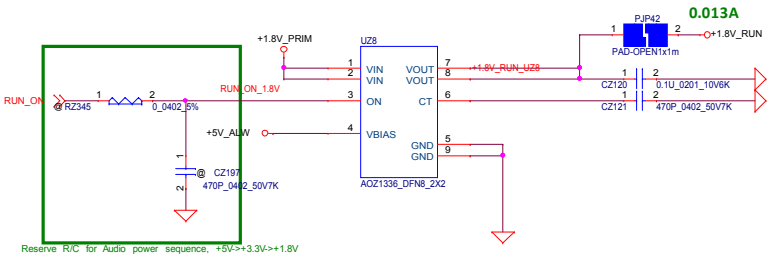
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File	Document Number	Rev
PAD_LED	LA-F391P	02
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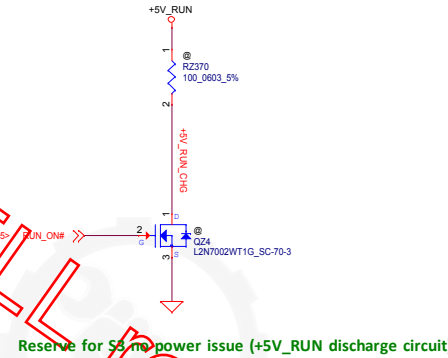
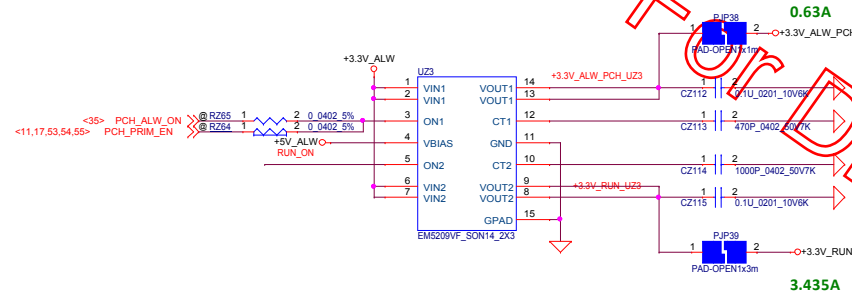
+3.3V_WWAN/+3.3V_LAN source



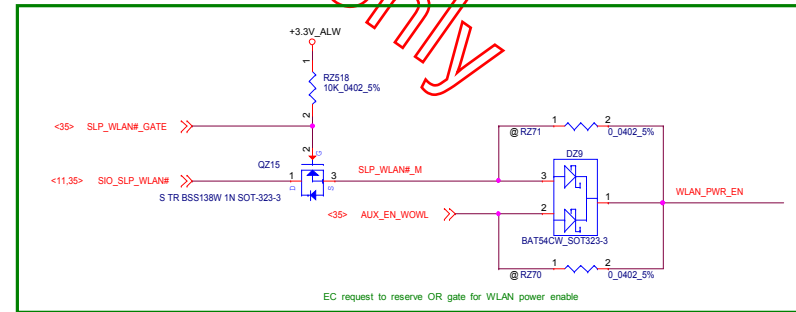
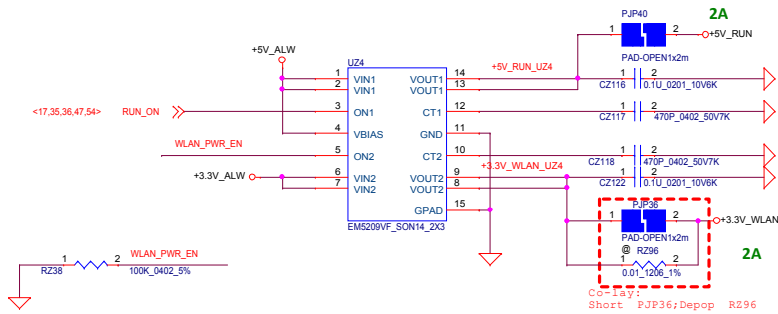
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source



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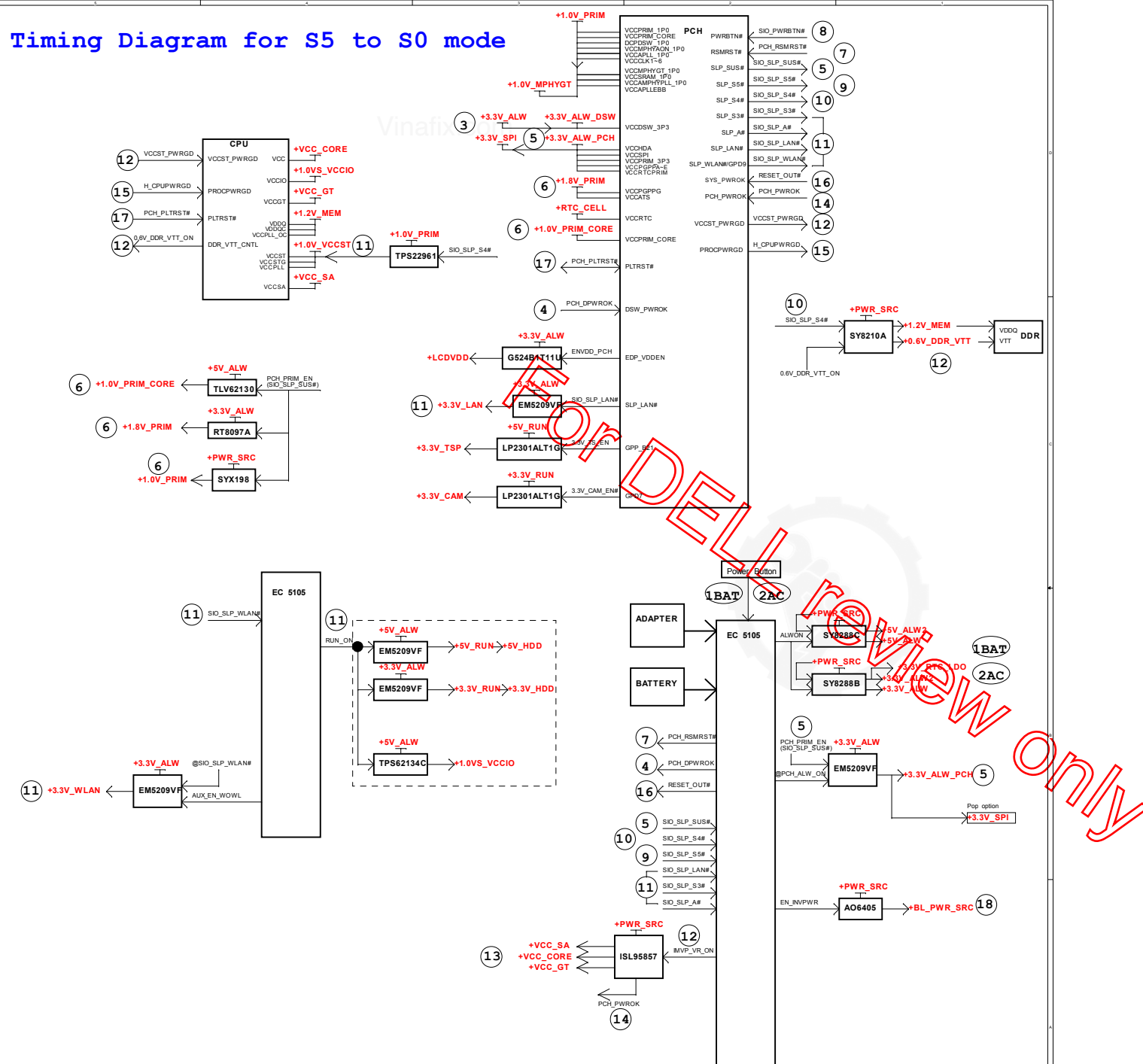
Power control

LA-F391P

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Timing Diagram for S5 to S0 mode



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Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay time(ps/inch)	25 ± 2.5 ohm single-end	35 ± 3.5 ohm single-end	39 ± 3.9 ohm single-end	43 ± 4.3 ohm single-end	45 ± 4.5 ohm single-end	48 ± 4.8 ohm single-end	50 ± 5 ohm single-end	52 ± 5.2 ohm single-end	50 ± 5 ohm Diff.	70 ± 7 ohm Diff.	75 ± 7.5 ohm Diff.	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref	90 ± 9 ohm Diff.	Ref		
			SolderMask	IT-158	0.5																															
			Add Plating																																	
1	Top		Copper foil	0.5oz+plating	1.6	149.18	13.4	8	6.6	5.5	5	4.4	4	3.7	13.5X	6.65.2	5.54.5	4.43.7	3.93.5	4.4.1	3.73.8				4.6	4.6.7	3.74.7	3.3.3	3.54.2	3.59.3	L.2	3.6.5	no Ref	3.6.5	L.3	
		3.8	Prepreg	1080	2.6		24.98	34.95	39.05	43.06	45.2	48.06	50.23	52	無法檢測	69.98	75	79.85	82.85	84.88	85.11				86.12	90.04	89.99	89.92	89.96	100.02		99.28		89.49		
2	GND		Copper foil	1oz	1.25										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
		3.7	Core	4mil	1.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
3	IN 1		Copper foil	1oz	1.25	161.77	11.4	6.6	5.6	4.7	4.3	3.7	3.5	3.3	11.4X	5.63.5	4.63.5	4.34.1	3.93.5	3.33.3	3.74.1	4.34.2	3.54.3	3.54.8	3.34.3	3.74.7		3.6.5	L.2/L.4	3.6.5	no Ref	3.6.5				
		3.7	Prepreg	2116H	4.1		24.92	34.99	39.12	42.94	44.9	46.22	49.45	51.84	無法檢測	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05		87.88	89.96	89.97	89.99		99.94		99.61				
4	GND/PWR		Copper foil	1oz	1.25										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
		3.7	Core	4mil	1.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
5	IN 2		Copper foil	1oz	1.25	166.76	10.5	6.3	7.7	6.5	5.6	5.2	4.6	4.4	15.51.2	7.75	6.64.6	5.53.7	4.63.6	4.4.3	4.43.8	3.34.3				4.64.2	4.65.9	4.44.7		4.07.0	L.4/L.7	4.3.5	no Ref	4.3.5		
		3.8	Prepreg	1080H x2 or P2116HRC	4.2		24.88	34.96	39.08	42.88	45.09	48.01	49.87	51.88	49.1	70.2	76.38	80.01	83.17	85.27	85.09	85.35				86.39	90.32	89.95		100.26		100.69				
6	IN 3		Copper foil	1oz	1.25		10.3	9.2	7.7	6.5	5.6	5.2	4.6	4.4	15.51.2	7.75	6.64.6	5.53.7	4.63.6	4.4.3	4.43.8	3.34.3				4.64.2	4.65.9	4.44.7		4.07.0	L.4/L.7	4.3.5	no Ref	4.3.5		
		3.7	Core	4mil	1.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
7	GND/PWR		Copper foil	1oz	1.25										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
		3.8	Prepreg	2116H	4.1		11.4	6.6	5.6	4.7	4.3	3.7	3.5	3.3	11.4X	5.63.5	4.63.5	4.34.1	3.93.5	3.33.3	3.74.1	4.34.2	3.54.3	3.54.8	3.34.3	3.74.7		3.6.5	L.7/L.9	3.6.5	no Ref	3.6.5				
8	IN 4		Copper foil	1oz	1.25		24.92	34.99	39.12	42.94	44.9	46.22	49.45	51.84	無法檢測	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05		87.88	89.98	89.97	89.99		99.94		99.75				
		3.7	Core	4mil	1.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
9	GND		Copper foil	1oz	1.25										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
		3.8	Prepreg	1080	2.6										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48								
10	Bottom		Copper foil	0.5oz+plating	1.6		13.4	8	6.6	5.5	5	4.4	4	3.7	13.5X	6.65.2	5.54.5	4.43.7	3.93.5	4.4.1	3.73.8				4.6	4.6.7	3.74.7	3.3.3	3.54.2	3.59.3	L.9	3.6.5	no Ref	3.6.5		
		3.8	Add Plating				24.98	34.95	39.05	43.06	45.2	48.06	50.23	52	無法檢測	69.98	75	79.85	82.85	84.88	85.11				86.12	90.04	89.99	89.92	89.96	100.02		99.75				
			SolderMask	IT-158	0.5																															
Overall Thickness (1.2mm ± 10%)					47.68000																															
					1.211072																															

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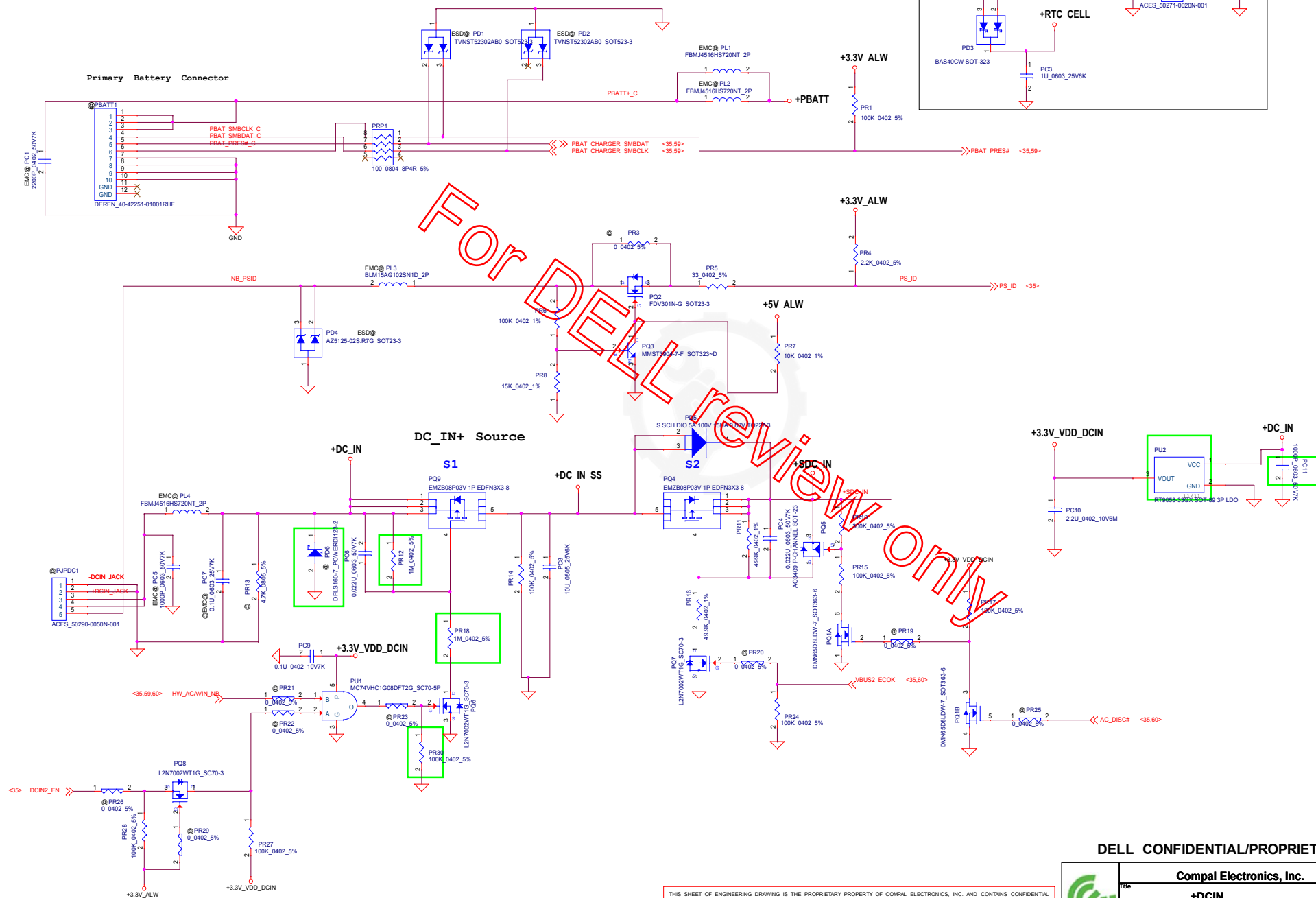
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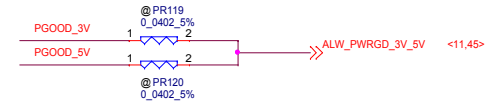
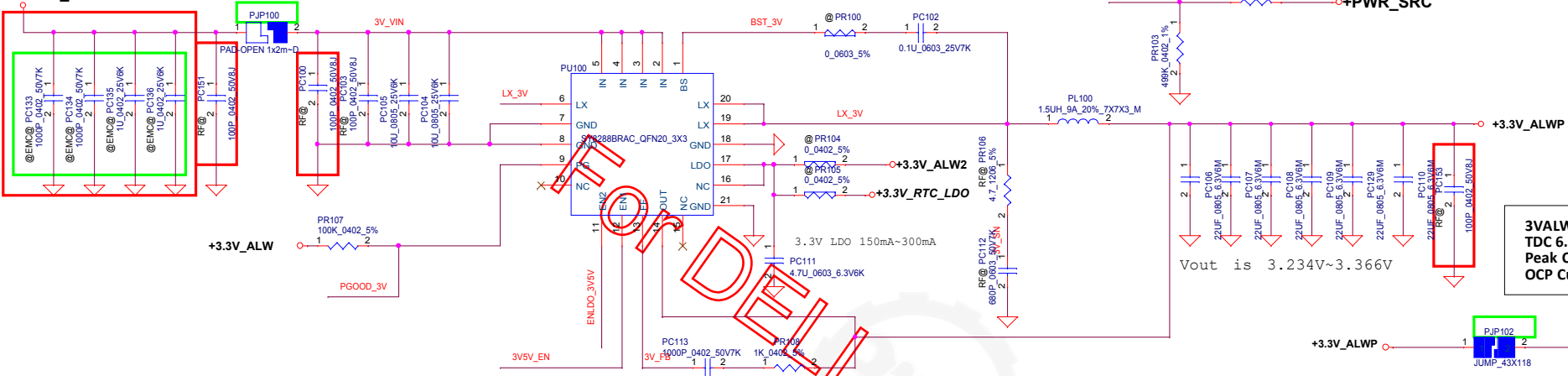
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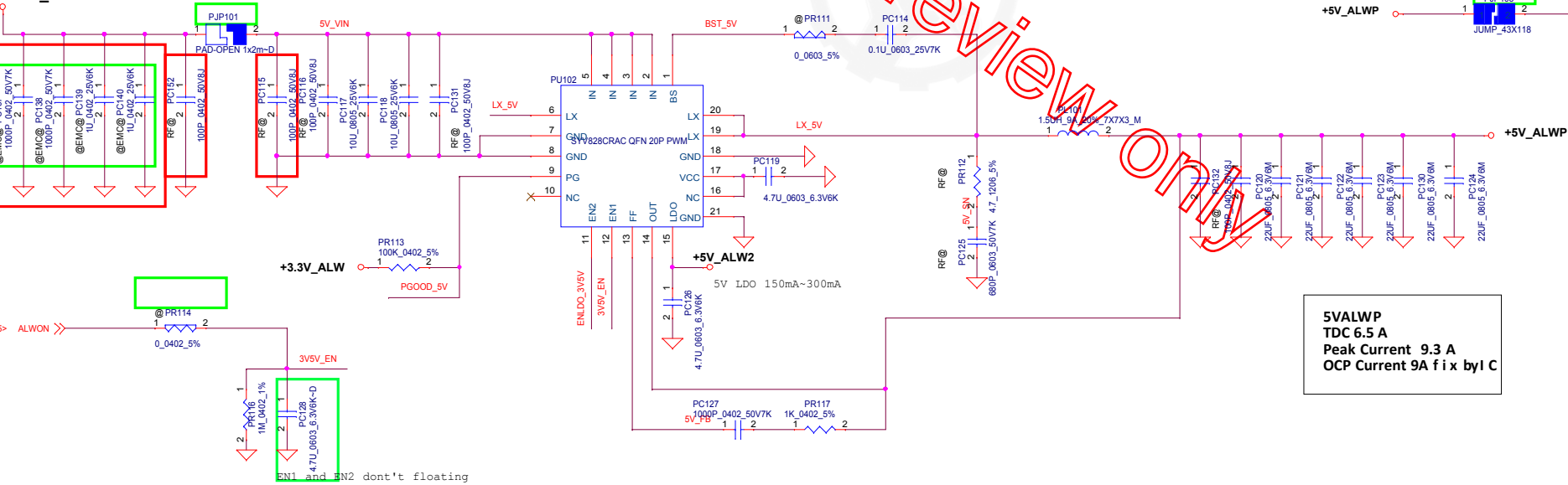
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3VALWP
TDC 6.8 A
Peak Current 9.7 A
OCP Current 9A fix by IC

Vout is 3.234V~3.366V

+3.3V_ALW

+5V_ALW

+PWR_SRC

5VALWP
TDC 6.5 A
Peak Current 9.3 A
OCP Current 9A fix by IC

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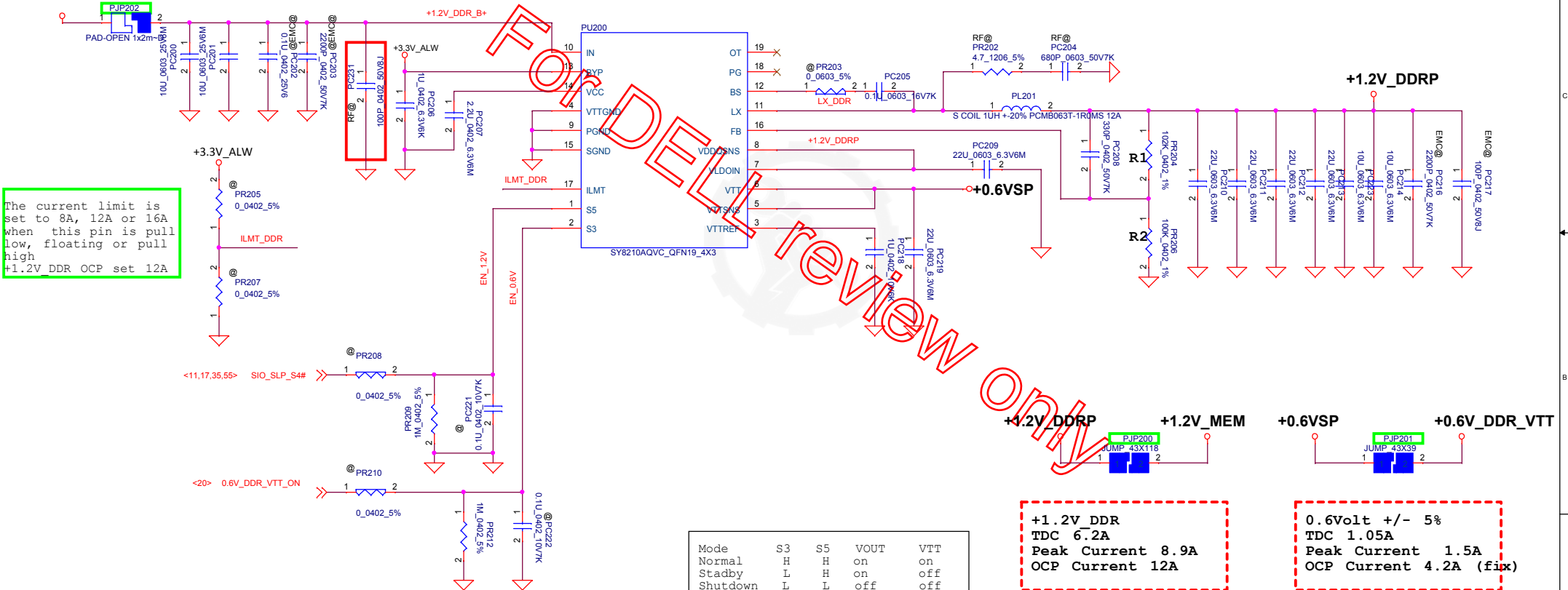
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+PWR_SRC



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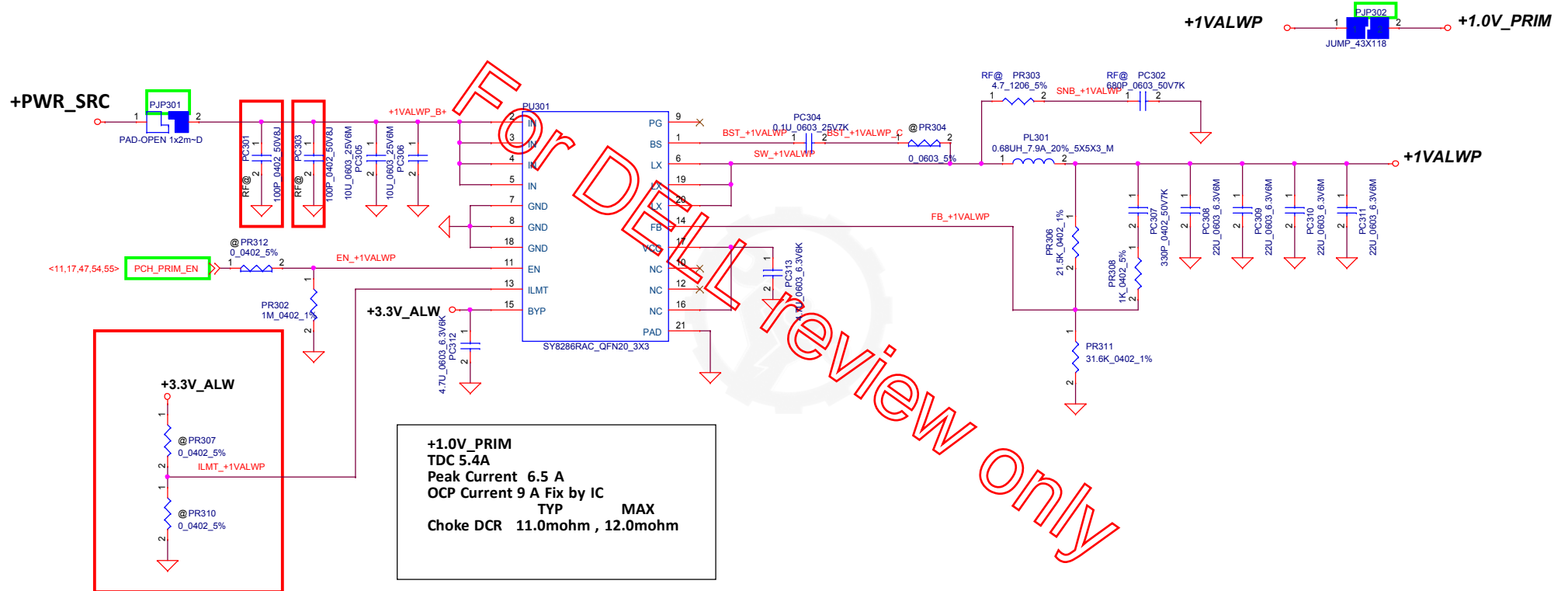


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Title
+1.2V_MEN/+0.6V_DDR_VTTSize Document Number
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The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

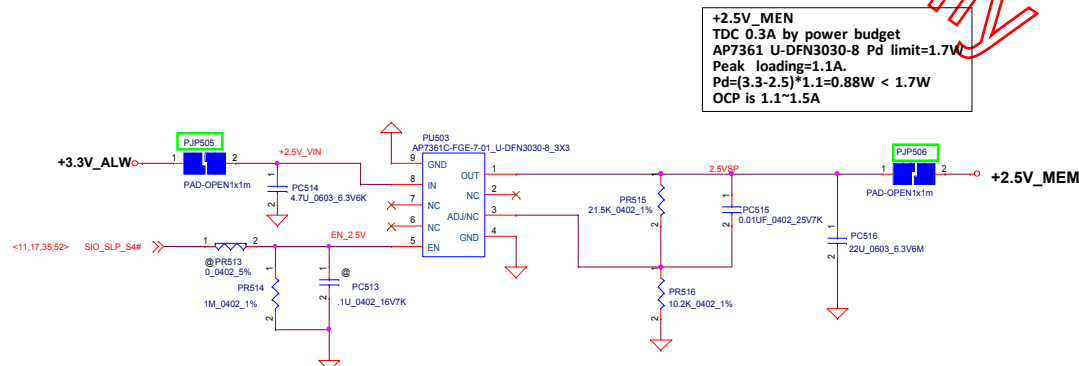
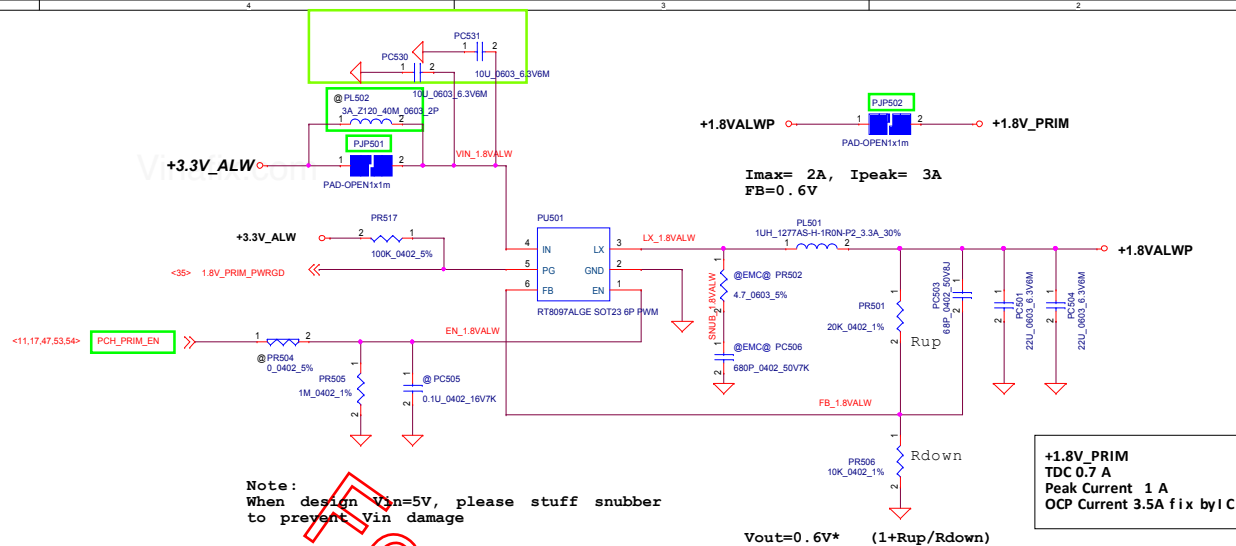
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		Compal Electronics, Inc.	
		+1.8VALWP/+1.2V_RUN/2.5V_MEM	
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Local sense put on HW site

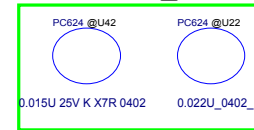
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VCC_SA U22
TDC 4.0A
Peak Current 4.5A
OCP current 10A
Choke DCR 6.2 m ohm

VCC_SA U42
TDC 4.0A
Peak Current 5A
OCP current 10A
Choke DCR 6.2 m ohm

VCCSA_B+ CPU_B+
PAD-OPEN1x1m

For ISUMN_IA Setting



VCCSA_B+

+VCC_SA

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ISUMP_VSA

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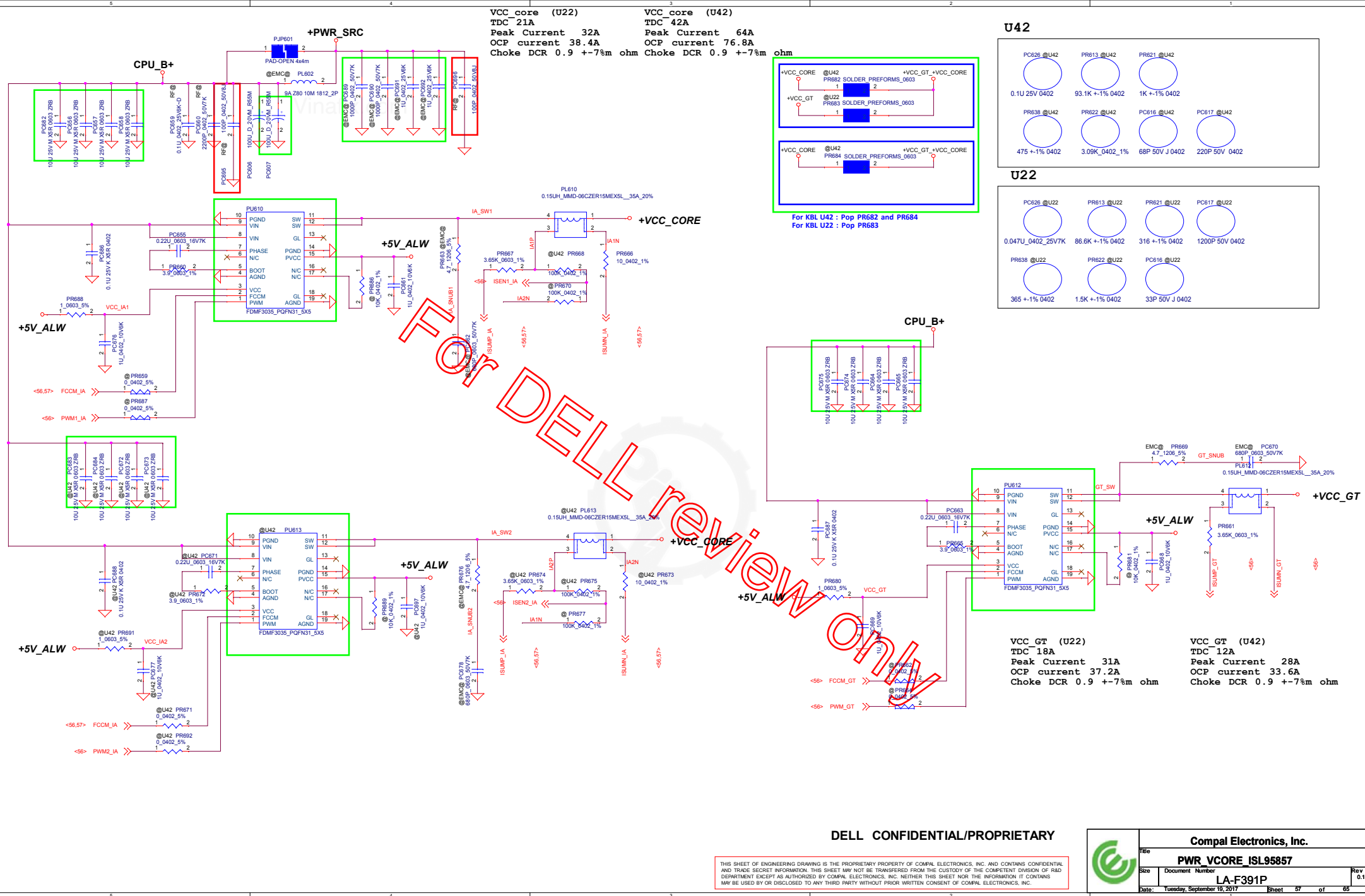


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PWR_VCORE_ISL95857

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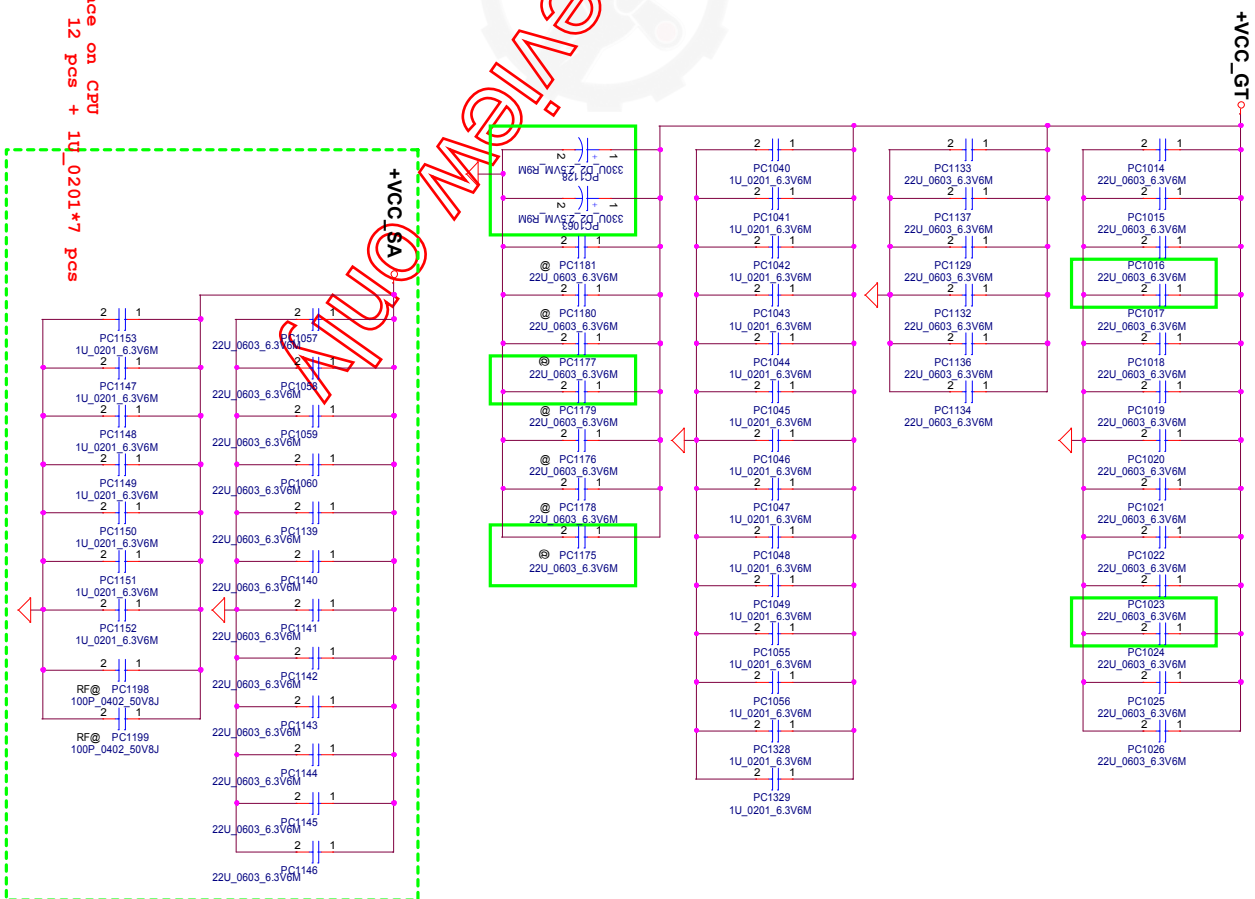
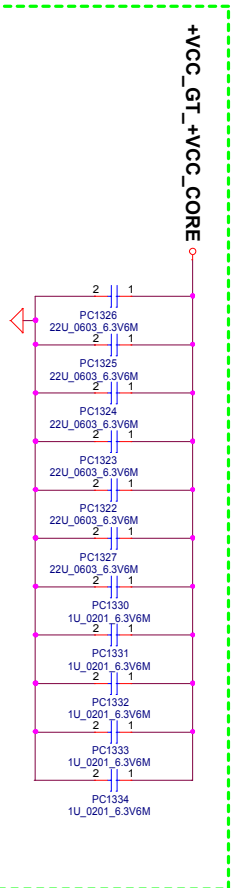


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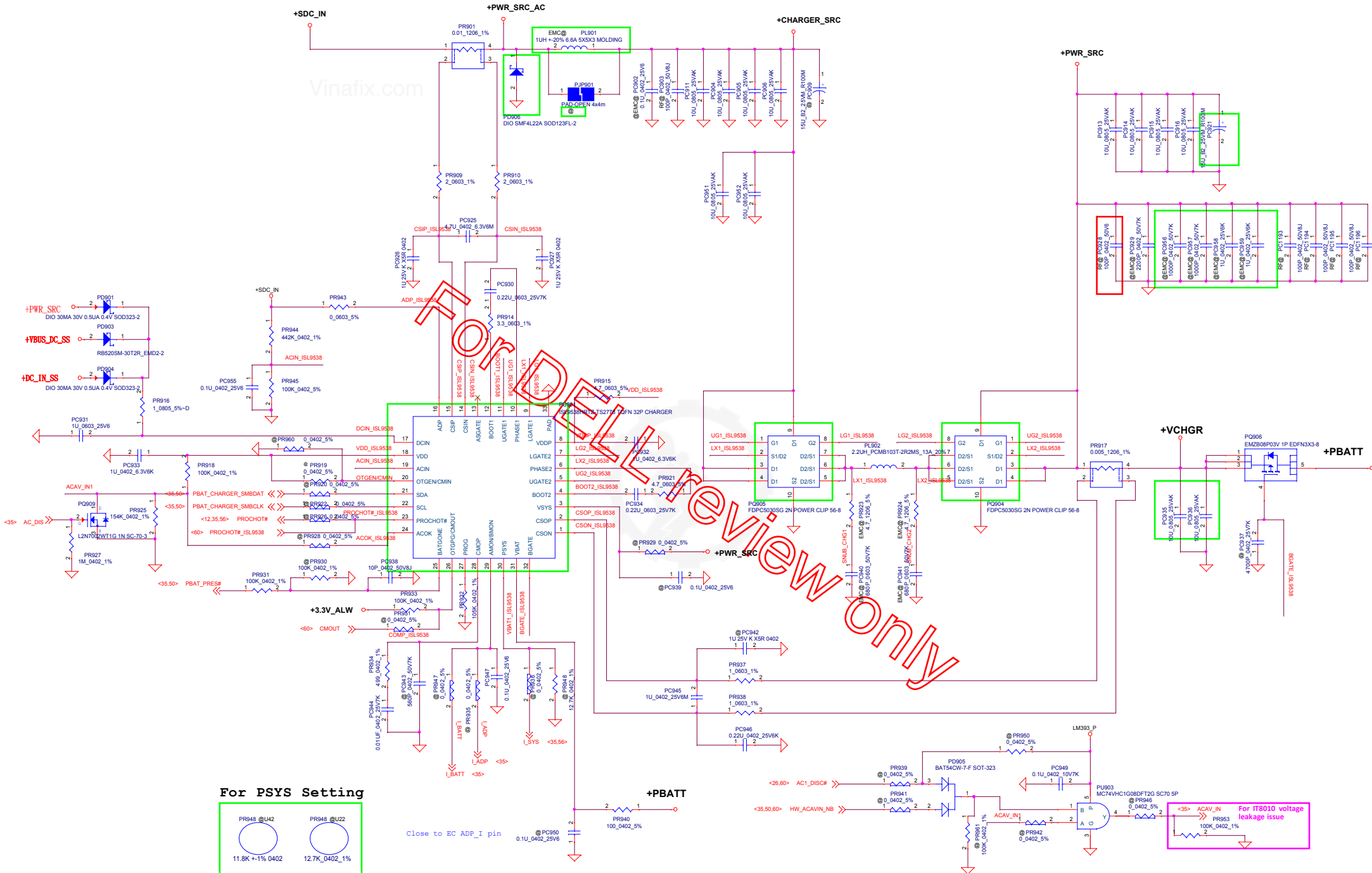
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VCC GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+220u_D7*2 pcs
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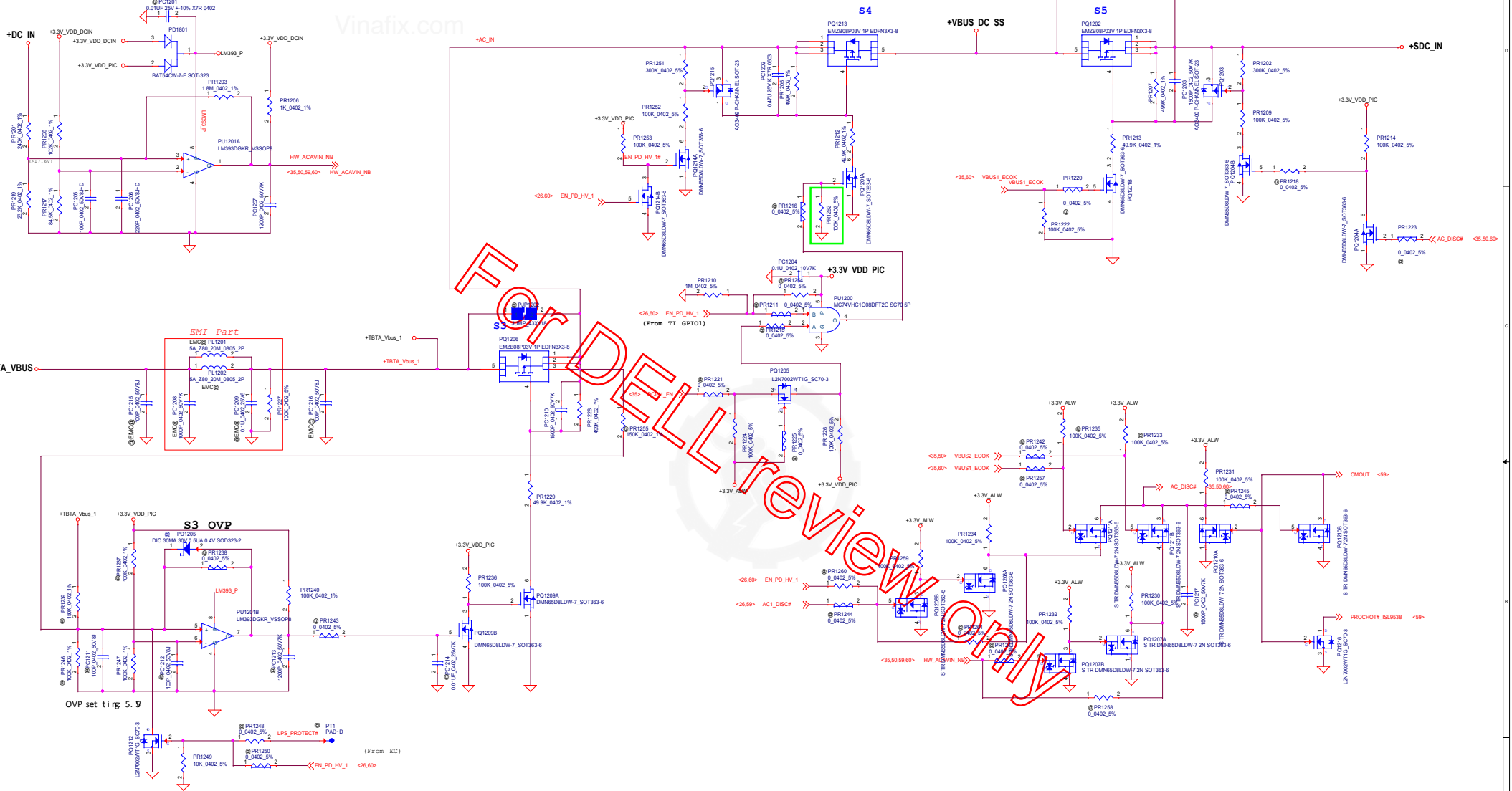
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		PWR charger_ISL9538	
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DCIN_AC_Detector

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Breckenridge TypeC PD	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	53 54 56 57	Add RF team portion	2017 04/06	Compal	RF request & modify Components	RF pop PC100,PC103,PC115,PC116,PC131,PC132,PC151,PC152,PC153,PC231,PC301,PC303,PC409,PC418,PC695,PC696,PC903,PC928,PC1191,PC1192,PC1193,PC1194,PC1195,PC1196	X00
2	58	Change DrMOS	2017 06/08	Compal	Change DrMOS from TI to Fairchild	DrMOS change from CSD97396 to FDMF3035	X01
3	51 57 59	Add EMI portion	2017 06/09	Compal	EMI request & modify Components	1. Depop PC133, PC134, PC135, PC136, PC137, PC138,PC139,PC140, PC689, PC690, PC691, PC692, PC956, PC957,PC958, PC959 2. Pop PL901.	X01
4	53 54 56 57	Add RF team portion	2017 06/13	Compal	RF request & modify Components	RF pop PC1198,PC1199	X01
5	56 57 59	Acoustic solution	2017 06/13	Compal	For acoustic solution CPU input MLCC change to 0603 low noise MLCC	1. Remove PC917, PC918, PC919, PC920 , add PC921 B2 POS CAP 2. CPU input MLCC size change from 0805 to 0603 low noise MLCC PC608, PC612, PC656, PC657, PC658, PC664, PC665, PC672, PC673, PC674, PC675, PC682, PC683, PC684 3. Pop PC607	X01
6	59	Change Charger Dual-MOS	2017 06/13	Compal	Change Dual-MOS from TI to AOS	Dual-MOS change from CSD87351 to AOE6936	X01
7	60	EMI portion	2017 07/28	Compal	EMI request & modify Components	Type-C PD Bead EOL ,so change BR_MLK12_14_15 PL1201/PL1202 Bead to 80 ohm bead, Change SM01000P200 to SM01000U400	X02
8	ALL	Change MLCC PN	2017 07/31	Compal	Change MLCC P/N L-end to 0-end	0-end P/N for all MLCC cap	X02
9	59	Add Charger portion	2017 08/03	Compal	Intersil FAE request PSYS Setting	For ISL9588 PSYS Setting PR948 change value 1.UMA U42 change from SD034127280(12.7kohm) to SD034118280 (11.8kohm) 2.UMA U22 keep SD034127280(12.7kohm)	X02
10	59 61	Change Charger portion	2017 08/11	Compal	Change current sense for component derating by Intersil FAE confirm	PR937,PR938,PR909,PR910,PR915 change 0402 to 0603 SD00001QK80	X02
11	ALL	0 ohm short pad	2017 08/11	Compal	Ohm change to 0 ohm short pad	For 0ohm no short pad: U42 DSC:Keep PR943,PR421,PR671,PR692 pop SD028000080	X02
12	59	Change Charger portion	2017 08/11	Compal	Power request	Add PD906 SC40000EL00 before PL901 Isum choke (SC40000EL00- S ZEN DIO SMF4L22A SOD123FL-2)	X02
13							

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13	56	IMVP8 CPU Controller Portion	2017 08/11	Compal	Intersil FAE request	Tune value for ISL95857A R,C match U42 1. Change PC624 SE068103K80 to SE075153K80 (0.015uF) 2. Change the PR629 from 86.6kOhm to 88.7kOhm. (IMON of GT) 3. Change the PC642 from 0.033uF to 0.022uF. (RC Match of GT) U22 1. Change PC624 SE068103K80 to SE076223K80 (0.022uF) 2. Change the PR638 from 383 Ohm to 365 Ohm	X02
14	59	Change Charger portion	2017 08/11	Compal	Buyer request	PD901,PD904 change from SCS0340L010 to SCS00009P00, for common part	X02
15							
16							
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1	40	M2 2280 Socket	2017/03/9	EE	For align with spindle HDD.	Add UZ37 circuit for 2280 SSD imdenpenden loadswitch --> add CN50~51, UZ37, PJP30_1*2(and no stuff all)	0.1(X00)
2	All	All	2017/03/9	EE	X9 request	UC1 CPU change from U22 to U42.	0.1(X00)
3	11	CPU (6/14)	2017/03/14	EE	KBL-R U42 X'tal	Add RC417~RC422,CC334,CC335, YC3 for U42 crystal	0.1(X00)
4	34	USH & TPM	2017/03/17	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
5	All	All	2017/03/17	EE	Remove IO expander	1-1.Delete expander IO UE2 relating circuit(RE524,@RE525 change to 0 ohm) remove UE2, CE1, CE2, RE13~18, RE6, CE500, CE504, CE505 4/13 add UMA RE524/525(2.2kohm)--> B6/F7 4/17 B6/F7 change netname to GPU_SMDAT/CLK 1-2. GPIO change (RE374 reserve) PCH RSMRST# GPIO204 -> USH PWR STATE# (delete RE363) PORT80 DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD IO3 -> VBUS1_ECOK (delete RE366~RE373, RE376,RE377,RE98,UE9) SHD IO1 -> SATA_LED_EN ENVDD PCH -> DCIN2_EN SIO RCIN# EC -> VBUS2_ECOK 1-3 For DSC (keep RE524, RE525)change name GPU_SMDAT/GPU_SMCLK SIO_EXT SCI# EC -> GPU_PWR_LEVEL (delete RE341) EXPANDER GPU_SMCLK -> DGPU_PWROK RTCRST_ON GPIO141(B6) -> GPU_SMDAT X(F7) -> GPU_SMCLK	0.1(X00)
6	36	MEC5105 Support	2017/03/24	EE	Remove Reset Threshold circuit	1. Delete UE7 relating circuit. keep RE536 only remove UE7, QE13, RE34, RE348, RE536, RE537, RE530 CE5, CE6, CE503 add RE536 on EC side	0.1(X00)
7	All	All	2017/03/24	EE	Add RTC reset circuit	1. RTCRST_ON GPIO122 change to RTCRST_ON... 2-1. +RTC_CELL_PCH circuit (Dell request) Delete RE514,RE515... Add QE14,QE17... Add RE540~RE546... Add CE63... Change RC56.2 net name to +RTC_CELL_PCH... Change UC1.AK19, UC1.BB14 net name to +RTC_CELL_PCH... 2-2.based on AR013 增加 R TC circuit 增加 B51避免+RTC_CELL_PCH 3. +3.3V_ALW_DSW enable circuit (Dell request) Delete RE524... Add RC431~RC433... Add UC13,UC14... Change UE1.M7 net name to VCCDSW_EN_GPIO... 4. GPIO change USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBDAT Delete RTCRST_ON GPIO141 PRIM_PWRGD GPIO024 -> RESET_IN# 5. UC13 chante to QC6, UC14 change to QC7 4/17 RTC power Gate circuit rev.2 Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)

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8	All	All	2017/03/14	EE	co-lay DS3/non-DS3	1. DS3 / non-DS3 co-lay Add DC2, (DC1 add NDS3 @) Add RC501, RC503, RC505 for DS3 Add RC502, RC504, RC506 for Non-DS3 Use the original 0ohm, RC215 instead of RC504, RE536 instead of RC503 3/14 1. based on EDS that add RC503 / RC504 on SUSACK # / ME_SUS_PWR_ACK for DS3 2. UZ3 enable pin change netname to PCH_PRIM_EN 3. RE349 + DS3 @ 4. UZ34 input in form SIO_SLP_SUS # to PCH_PRIM_EN 3/15 1. For align KW that change as below "Part Reference" A RC501 -> RC439 B. RC502 -> RC440 C. RC503 -> RC443 D RC504 -> RC444 E. RC505 -> RC441 F RC506 -> RC442 3/27 Parallel 0ohm in DC2, reserved to avoid NDS3 @, EC too late to load code 4/17 RTC Power Gate Circuit option RC445 change to connect to VCCDSW_EN and pop	0.1 (X00)
9	09	CPU (4/14)	2017/03/27	EE	For antenna request	1. Add RC434, RC435 0ohm for JUART1 power option 4/17 JUART whether pin swap, Align with SB. --> Pin swap align SB --> EVT phase pop JUART, DVT phase remove 4/20 2. Remove RC435	0.1 (X00)
10	38	USH & TPM	2017/03/27	EE	Prevent contactless_det# backdrive	1. Add DZ8 to prevent contactless_det# backdrive	0.1 (X00)
11	37	USH & TPM	2017/03/15	EE	TPM650 include	1. TPM a. Delete RZ113, RZ111, QZ9 b. Add RZ365 and connect to +UZ12_TPM Add RZ366 and connect to +3.3V_M_TPM	0.1 (X00)
12	13	CPU (8/14)	2017/03/15	EE	Follow CRB	UC1.F65 & G65 to GND add RC436 to GND before UC1.F65 & G65	0.1 (X00)
13	16	CPU (11/14)	2017/03/15	EE	Follow MOW08	UC1.K52/AK52 Must be NOT connected	0.1 (X00)
14	10	CPU (5/14)	2017/03/28	EE	X9 Port MAP check	1. USB3.0 port1 with port6 swap 2. USB2.0 port1 with port9 swap	0.1 (X00)
15	9	CPU (4/14)	2017/03/29	EE	For Layout power trace	add +UART1_R power netname on JUART1	0.1 (X00)
16	8	CPU (3/14)	2017/03/29	ME	Connector check	JSPI1 change from ENTERY_SP01001FW00 to ACES_SP01001CB10	0.1 (X00)
17	31,11	Card Reader RTS5242 CPU (6/14)	2017/03/29	EMI	EMI request	1. RR5~RR10 change to 0ohm 2. RC417~RC420 change from 0ohm to 33ohm	0.1 (X00)
18	28	USB 3.0 CONN TYPE C	2017/03/29	ESD	ESD request	1. Change DT7, DT8, DT11, DT12 to DT39 2. Change DT15, DT16, DT19, DT20 to DT40	0.1 (X00)

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19	16	CPU (11/14)	2017/03/29	EE	For BRMLK12 layout request	Let AK70,BB57,BB66,AU58,AU63 floating	0.1(X00)
20	All	All	2017/03/31	EE	Follow ARD1.3 remove WIGIG	1-1.change Source 1:3 demultiplexer(PS8348B) to 1:2 demultiplexer(PS8338B) 1-2,remove RV71, RC74, RV77, CV80 2-1. (DP)JNGFF1 remove CV145~150, CV152, CV153, CV156, CV157 2-2. (PCIE)JNGFF1 remove CZ14, CZ15 UC1 remove RC375	0.1(X00)
21	37	USH & TPM	2017/03/31	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
22	35	EC MEC5105	2017/04/05	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
23	8	CPU (3/14)	2017/04/05	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
24	26	[Type C]PD Controller TI	2017/04/05	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
25	36	MEC5105 Support	2017/04/05	EE	Board ID define change	change RE79 to 240K for X00	0.1(X00)
26	All	All	2017/04/05	EE	EC GPIO check	1. rename form AUD_NB MUTE# to NB MUTE# for EC team request 2. rename form SYS_LED MASK# to LED MASK# for EC team request 3. change net name form THERMATRIP1# to THERMTRIP1# for EC team request 4. swap WWAN RADIO DIS# from UE1.M2 to UE1.F12 5. swap LCD TST from UE1.D1 to UE1.M2	0.1(X00)
27	All	All	2017/04/06	EE	EC GPIO check	1. rename form FAN1 TACH to TACH FAN1 for EC team request 2. DSC swap DGPU PWR_EN to GPIO100 for save level shift at BR MLK project 3-1. DSC swap GPU PWR LEVEL to GPIO126 for save level shift at BR MLK project 3-2. DSC remove RE5 of GPIO126, 3-3. UMA remove RE341 of SIO EXT SCI# 4. SYS PWROK reserved 0ohm add netname to RESET_OUT 5. rename form ME FW_EC to ME FWP for EC team request 6. rename from ME FWP to ME FWP PCH 7. rename from HW GPS DISABLE# to GPS DISABLE# for EC team request 8-1. rename from VGA_ID to VGA IDENTIFY for EC team request 8-2. swap to GPIO035 form GPIO017 for ECTeam suggestion BEEP need change to PWM function 8-3. Swap BEEP pin to GPIO035 form GPIO017 EC team request. 9. rename from H PROCHOT# to PROCHOT# for EC team request 10. rename from USB_PWR_SHR_VBUS_EN to USB_POWERSHARE_VBUS_EN for EC team request	0.1(X00)
28	47	Power control	2017/04/07	EE	+5V_RUN discharge circuit for S3 no power issue	1. Add but not stuff Q24 and R2370 2. Add zener diode DE1 (no stuff) for + 5V_RUN discharge 3. RZ370 into 0603 packaging, add net name	0.1(X00)
29	8	CPU (3/14)	2017/04/07	ME	JSP11 footprint pin1 Reversal 180 of ENTERY to ACES	Symbol reverses 180 degrees	0.1(X00)
30	24	DP to VGA & VGA Conn	2017/04/07	EE	When the system can not read the VGA EDID, the maximum resolution will be pressed at 1024x768	reserve RV620 PU to +3.3V_RUN ** Pop RV620	0.1(X00)
31	36	MEC5105 Support	2017/04/07	EE	To increase power current rail for each debug card	RE71 changed to SD034100A80, that change 49.9 to 10ohm current limiting resistor to smaller.	0.1(X00)

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32	All	All	2017/04/07	EE	EC GPIO check	1. rename from USB_PWR_SHR_LFT_EN# to USB_POWERSHARE_EN# for EC team request	0.1 (X00)
33	All	All	2017/04/10	EE	EC GPIO check	1. 3.3V TS_EN rename to PCH_3.3 TS_EN SHD_IO0 change to 3.3V TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V TS_EN/PCH_3.3V TS_EN option 2. SHD_CLK -> PS_ID and delete RE374 3. CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 4. change net name form PANEL_ID to SYSTEM_ID 5. SIO_EXT_SMI#_EC -> free and delete RE338 6. SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 7. rename from SATA_LED_EN to MASK_SATA_LED# for EC team request 8. rename form FAN1_PWM_1 to PWM_FAN1 for EC team request 9. GPIO054 (PS_ID) swap to GPIO056 for EC team request 10. PCH_ALW_ON keep GPIO231 and assign DCIN2_EN to GPIO107 11. EXPANDER_GPU_SMCLK -> free and delete RE525 12. this pin should be change to reserved, Current EC no use PCH_ALW_ON to control +3.3V_ALW_PCH, it control by SIO_SLP_SUS# directly 13. rename from SLOT2_CONFIG_1 to NGFF_CONFIG_1 for EC team request 14. rename from ACAV_IN_NB to HW_ACAVIN_NB for EC team request 15. rename from SLOT2_CONFIG_0 to NGFF_CONFIG_0 for EC team request 16. rename from SLOT2_CONFIG_2 to NGFF_CONFIG_2 for EC team request 17. rename from LID_CL_NB# to LID_CL_SIO# for EC team request	0.1 (X00)
34	All	All	2017/04/11	EE	PCH GPIO check	1. Follow SB reserve CLKDET# net, for x7~x8 no use 2. Follow SB reserve CLKRUN# net, for no use LPC mode 3. DEL SIO_RCIN# net, for no use LPC mode 4. Follow SB reserve SIO_EXT_SCI#, for no use LPC mode 5. Rename PCH_3.3V_TS_EN from 3.3V_TS_EN 6. Follow SB reserve PCI_CLK_LPC1, for no use LPC mode 7. Follow SB reserve PME#, for no use LPC mode 8. Follow SB reserve SIO_EXT_SMI# net, for no use LPC mode	0.1 (X00)
35	All	All	2017/04/11	EE	Following port MAP	BOM port to be replaced to port 4	0.1 (X00)
36	All	All	2017/04/13	EMI	EMI request	change 0ohm short pad to 0ohm of as below. RC328, RT54-57, R256, RN99	0.1 (X00)
37	All	All	2017/04/17	EE	For All of Repeater	4/17 PWD pin setting double check for all of redrive (dual, signal, USB3) 4/21 UMA 1. SATA repeater --> add QN6, RN226, RN227 2. PCIE/SATA repeater --> add QN7, RN228, RN229, RN230 DSC 1. PCIE/SATA repeater --> add QN6, RN226, RN227	0.1 (X00)
38	All	All	2017/04/17	EE	GPIO map change	4/17 PCH_3.3V_TS_EN PU +3.3V_RUN change page to QV7.2 --> Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN 1. RC443 BOM structure change to @ 2. UMA : GPIO126->GPU_PWR_LEVEL 3. Add RTCRST_ON_R net name for QE17.2 4. Add SIO_SLP_SUS# R net name and PU RE561 5. RC27.2->NC for CLKRUN# 6. UMA : HDD_DET#->SATAGP0 7. Remove RE360/RE364 .	0.1 (X00)

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39	47	Power control	2017/04/19	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9 4/20 RZ38 PD change to WLAN_PWR_EN_UZ2	0.1 (X00)
40	36	MEC5105 Support	2017/04/19	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1 (X00)
41	All	All	2017/04/19	EE	OTG support	Pop RT74, Depop RC337 4/20 RC337 10K to GND	0.1 (X00)
42	35	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->GPIO202 Add test point T147 for UE1.M4->DGPU_PWROK only UMA	0.1 (X00)
43	38	USH & TPM	2017/04/19	EE	JUSH1 add net name	1. Add net name at DZ8.1 .	0.1 (X00)
44	37	USH & TPM	2017/04/21	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1 (X00)
45	37	USH & TPM	2017/04/24	EE	BOM option by " 6500" or " 7500"	1.The pop option for VHIO power: NPCT750: VHIO=+3.3V RUN NPCT650: VHIO=+3.3V_ALW_PCH 2.The pop option for SLP_S0# connection: NPCT750: pop RZ112 (SLP_S0#=GPIO0) NPCT650: pop RZ363 (SLP_S0#=GPIO2) 3.RZ62 can be removed	0.1 (X00)
46	9	CPU (4/14)	2017/04/24	EE	JUART1 remove	remvoe JUART1, RC434	0.1 (X00)
47	11	CPU (6/14)	2017/04/24	EE	Schematic align	INTRBUDR# PU change to +RTC_CELL_PCH	0.1 (X00)
48	All	All	2017/04/24	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#-->UPD1_SMBINT# UPD1_SMBUS_ALERT#-->UPD1_SMBINT#_R	0.1 (X00)
49	34	Codec ALC3253	2017/03/31	EE	Follow ARD1.3 change Codec to 3254	Change Codec schematic from ALC3253 to ALC3254	0.1 (X00)
50	34	Codec ALC3253	2017/04/13	EE	Swap ESD diode pin for layout	DT39 & DT40 swap pin	0.1 (X00)

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32	All	All	2017/04/07	EE	EC GPIO check	1. rename from USB_PWR_SHR_LFT_EN# to USB_POWERSHARE_EN# for EC team request	0.1 (X00)
33	All	All	2017/04/10	EE	EC GPIO check	1. 3.3V TS_EN rename to PCH_3.3 TS_EN SHD_IO0 change to 3.3V TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V TS_EN/PCH_3.3V TS_EN option 2. SHD_CLK -> PS_ID and delete RE374 3. CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 4. change net name form PANEL_ID to SYSTEM_ID 5. SIO_EXT_SMI#_EC -> free and delete RE338 6. SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 7. rename from SATA_LED_EN to MASK_SATA_LED# for EC team request 8. rename form FAN1_PWM_1 to PWM_FAN1 for EC team request 9. GPIO054 (PS_ID) swap to GPIO056 for EC team request 10. PCH_ALW_ON keep GPIO231 and assign DCIN2_EN to GPIO107 11. EXPANDER_GPU_SMCLK -> free and delete RE525 12. this pin should be change to reserved, Current EC no use PCH_ALW_ON to control +3.3V_ALW_PCH, it control by SIO_SLP_SUS# directly 13. rename from SLOT2_CONFIG_1 to NGFF_CONFIG_1 for EC team request 14. rename from ACAV_IN_NB to HW_ACAVIN_NB for EC team request 15. rename from SLOT2_CONFIG_0 to NGFF_CONFIG_0 for EC team request 16. rename from SLOT2_CONFIG_2 to NGFF_CONFIG_2 for EC team request 17. rename from LID_CL_NB# to LID_CL_SIO# for EC team request	0.1 (X00)
34	All	All	2017/04/11	EE	PCH GPIO check	1. Follow SB reserve CLKDET# net, for x7~x8 no use 2. Follow SB reserve CLKRUN# net, for no use LPC mode 3. DEL SIO_RCIN# net, for no use LPC mode 4. Follow SB reserve SIO_EXT_SCI#, for no use LPC mode 5. Rename PCH_3.3V_TS_EN from 3.3V_TS_EN 6. Follow SB reserve PCI_CLK_LPC1, for no use LPC mode 7. Follow SB reserve PME#, for no use LPC mode 8. Follow SB reserve SIO_EXT_SMI# net, for no use LPC mode	0.1 (X00)
35	All	All	2017/04/11	EE	Following port MAP	BOM port to be replaced to port 4	0.1 (X00)
36	All	All	2017/04/13	EMI	EMI request	change 0ohm short pad to 0ohm of as below. RC328, RT54-57, R256, RN99	0.1 (X00)
37	All	All	2017/04/17	EE	For All of Repeater	4/17 PWD pin setting double check for all of redrive (dual, signal, USB3) 4/21 UMA 1. SATA repeater --> add QN6, RN226, RN227 2. PCIE/SATA repeater --> add QN7, RN228, RN229, RN230 DSC 1. PCIE/SATA repeater --> add QN6, RN226, RN227	0.1 (X00)
38	All	All	2017/04/17	EE	GPIO map change	4/17 PCH_3.3V_TS_EN PU +3.3V_RUN change page to QV7.2 --> Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN 1. RC443 BOM structure change to @ 2. UMA : GPIO126->GPU_PWR_LEVEL 3. Add RTCRST_ON_R net name for QE17.2 4. Add SIO_SLP_SUS# R net name and PU RE561 5. RC27.2->NC for CLKRUN# 6. UMA : HDD_DET#->SATAGP0 7. Remove RE360/RE364 .	0.1 (X00)

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39	35	MEC5105 ESPI EC	2017/06/06	EE	GPIO map change	UPD2_ALERT#-->UPD2_SMBINT#	0.2 (X01)
40	47	Power control	2017/06/06	EE	Change netname align with SB	WLAN_PWR_EN_U2--> WLAN_PWR_EN	0.2 (X01)
41	16	MCP(11/14) PWR-VCCGT	2017/06/06	EE	Add netname for layout	RC437.2 --> +VCC_GT_K52 RC438.1 --> +VCC_GT_AK52	0.2 (X01)
42	47	MEC5105 ESPI Power control	2017/06/06	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Change SIO_SLP_WLAN# to SLP_WLAN#_GATE (EC side UE1.K10) & Add RE552	0.2 (X01)
43	26	[Type C]PD Controller TI-1	2017/06/06	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2 (X01)
44	11	MCP(6/14) CLK,PM,RTC	2017/06/07	EE	Schematic align, avoid SUSACK#_R floating	Reserve RC551	0.2 (X01)
45	37	NuvotonTPM1.2	2017/06/07	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM PIRQ# power rail change to +3.3V ALW_PCH Change UZ12 to SA0000AQ200 and related resistors	0.2 (X01)
46	24	DP to VGA & VGA ConnRTD2166	2017/06/07	EE	RTD2166 question	UV6.12 add RV622 PU to +3.3V_RUN	0.2 (X01)
47	28	[Type C]USB 3.0 CONN TYPEC1	2017/06/07	ESD	ESD request	DT10, DT13, DT14, DT17,DT18,DT5,DT6,DT9 change from SC40000AT00 to SC40000DF00	0.2 (X01)
48	33	NuvotonTPM1.2	2017/06/07	EE	For RBOM request.	CZ75 from 4.7uF to 10uF	0.2 (X01)
49	33	NGFF Card	2017/06/07	EE	Correct the symbol	Update JNGFF1/JNGFF2 symbols	0.2 (X01)
50	20,36	All	2017/06/08	EE	Main source change	UD1, UE4, UE6 change to SA00007WE00	0.2 (X01)
51	46	All	2017/06/08	DFB	DFB request	PCB hole from 3.2mm to 3.3mm Location:H34,H35 LA13 symbol change to " TAI-T_HCB2012KF-121T50_2P"	0.2 (X01)
52	ALL	All	2017/06/12	DELL	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2 (X01)
53	36	MEC5105 Support	2017/06/14	EE	BOARD_ID change	Change REV to 130Kohm (rev. X01)	0.2 (X01)
54	30	LAN	2017/06/14	EMI	EMI request	add +0.9V_LAN LL2 180 ohm bead	0.2 (X01)
55	29	DMIC	2017/06/14	RF	RF request	CA5,CA6 change to 27pf	0.2 (X01)
56	41	All	2017/06/15	DELL	DELL request	1-1. pop PJP33 1-2. Non-pop UZ23,CZ129,CZ130,PJP32 2-1. del UZ37,CN50,CN51,PJP30	0.2 (X01)
57	9	MCP(4/14)GSPI ,I2C,UART,ISH	2017/06/15	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2 (X01)
58	47	Power Control	2017/06/15	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2 (X01)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
59	41	All	2017/06/15	DELL	DELL request	1-1. pop PJP33 1-2. Non-pop UZ23,CZ129,CZ130,PJP32 2-1. del UZ37,CN50,CN51,PJP30	0.2 (X01)
60	9	MCP(4/14)GSPI,I2C,UART,ISH	2017/06/15	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2 (X01)
61	47	Power Control	2017/06/15	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2 (X01)
62	25	DP/USB Redriver SW1 TUSB546	2017/06/15	EE	PS8743 colay	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213 Add RT405, RT406, RT407, RT417, RT418	0.2 (X01)
63	30	Codec - ALC3246	2017/06/16	EMC	EMC request	CL11,CL12 change to close UL1.46,47	0.2 (X01)
64	24	DP to VGA & VGA ConnRTD2166	2017/06/21	EE	RTK suggest	LV19/LV20 --> RV650/RV651 改5 Ω ; CV132/CV133 改P	0.2 (X01)
65	26	[Type C]PD Controller TI-1	2017/06/21	EE	TPS65982 (UT5) update version	DB --> DC (SA0000AX700)	0.2 (X01)
66	34	Codec ALC3246	2017/07/26	ESD	ESD request	DA2, DA6, DA7 change main source from SCA00002900 to SCA00001A00	0.3 (X02)
67	ALL	All	2017/08/01	EE	Change cap to 0-end P/N	0-end P/N for all cap	0.3 (X02)
68	26	[Type C]PD Controller TI	2017/08/02	EE	TI TPS65982 request(TBTA_DEBUG4)	pop RT407 when pop 8743 & change to 10K	0.3 (X02)
69	28	USB 3.0 CONN TYPE C	2017/08/02	EE	SE part COS issue.	CT99, CT100, CT101, CT102 change to 0.01u_X5R_0201_25V (SE000000YH00)	0.3 (X02)
70	25	DP/USB3 Repeater SW TUSB546	2017/08/02	EE	TI update version(TUSB546A)	TUSB546 change form SA00009R710 to SA00009R720	0.3 (X02)
71	ALL	All	2017/08/03	EE	To avoid in-rush current caused voltage drop	Add soft start solution(only reserved) on QV8,QZ1 (add CV635, CZ200, RZ380,RV400) 8/4 Add soft start solution(only reserved) on QE15,QC7 (add CC340,RE565)	0.3 (X02)
72	36	MEC5105 Support	2017/08/08	EE	BOARD_ID change	Change RE79 to 62Kohm (rev. X02)	0.3 (X02)
73	9	CPU (4/14)	2017/08/09	EE	TPM Pin connectivity requirement	Add RC560,RC561(reserved) BOM options.	0.3 (X02)
74	ALL	All	2017/08/11	EE	Buyer request	main source change 1 .SC1N4148180 --> SC100005500 2. SC100000S00 --> SCS000003700	0.3 (X02)
75	30	All	2017/08/11	EMI	EMI request	CL10 depop	0.3 (X02)

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